McIDAS
Man computer Interactive Data Access System

WIDE WORD Workstation
Hardware Manual
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Issued March 1991

Space Science and Engineering Center
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MclDAS
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WIDE WORD Workstation
Hardware Manual
(Serial numbers 32 and above)

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Revised 1992

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McIDAS WIDE WORD Workstation Overview

The McIDAS (Man computer Interactive Data Access System) WIDE WORD* Workstation (WWW) is the link between the user and McIDAS. It provides the animated display of satellite imagery and weather data. The workstation allows the user to issue commands to the McIDAS mainframe and receive digital image and graphics information from it. The WWW stores, processes and displays image and graphics data and displays this data on one or more color monitors. Users’ systems range from a single McIDAS workstation linked remotely to SSEC’s McIDAS, to complete systems like SSEC’s McIDAS, to more elaborate systems similar to SSEC’s McIDAS but with more or different components.

This overview provides:

- a brief description of SSEC’s McIDAS to show how the WWW fits into the total system
- a description of the components that make up a complete WWW
- a WWW functional description

* WIDE WORD is a logo of the Dataram Corporation.
Figure 1. Simplified SSEC McIDAS
McIDAS System Description

Figure 1 on the adjacent page is a block diagram of the SSEC McIDAS. Each block or group of blocks is described below in terms of its function within the system.

**POES, GOES and METEOSAT Data Antennas**

POES (Polar Orbiting Environmental Satellite), GOES (Geostationary Orbiting Environmental Satellite) and METEOSAT (European Meteorological Satellite) antennas receive image and sounder data signals from their respective satellites. These antennas receive signals in the VHF and microwave frequency spectra. Low noise amplifiers, down converters and demodulators associated with each antenna recover a modulation signal consisting of a composite of data and clock.

**Frame and Bit Synchronizers**

Each demodulated signal is processed by a Bit Synchronizer which separates the signal into a serial data stream and clock signal. The Bit Synchronizers send their outputs to a respective Frame Synchronizer which outputs a serial or parallel data format (depending on the signal type - POES, GOES, METEOSAT, etc.) to the Archive/Playbacks and Ingestors.

**Archive/Playbacks**

The Frame Synchronizers' outputs are stored digitally on video cassette cartridges. The playback unit allows previously recorded Frame Synchronizer outputs to be read into the system at any time for user analysis.

**Multisourcerer**

Inputs to and outputs from the IBM mainframe computer are via the mainframe's I/O channels. The Multisourcerer is an SSEC designed and built programmable interface between an IBM I/O Channel and up to six external devices (ingestors, etc.). It contains a seven-slot cardcage having an interface controller and six unused Multibus compatible board slots. SSEC has developed these three types of applications cards that can be plugged into a Multisourcerer:

- ingestors
- Local Area Network (LAN) controllers
- synchronous communications controllers

Because of the complexity of the SSEC McIDAS, several Multisourcerers are used. However, a single Multisourcerer may control all three types of applications cards simultaneously in a less complex McIDAS.
Ingestors

Each type of satellite has its own ingestor card. Currently, ingestors are available for:

- POES
- GOES Imaging
- GOES Sounding (2-card set)
- METEOSAT
- GMS (Japan’s Geosynchronous Meteorological Satellite)
- GOES Mode AAA Auxiliary Block

Ingestors receive serial or parallel data, clock and control signals from their respective Frame Synchronizer or Archive/Playback. The ingestors assemble the incoming data into complete scans or blocks of data. Upon command from the mainframe, the ingestors send requested frames or blocks (or parts of frames or blocks) to the mainframe via the Multisourcerer’s interface controller. The ingestors relieve the mainframe of much of the computing overhead associated with the ingest process.

IBM Mainframe Computer

The IBM mainframe computer (4381-14) receives imagery data from the ingestors via their Multisourcerer, and conventional meteorological data via the Communications Controller. The mainframe computer contains the operating system, applications programs and subroutines. It functions as a data processor, database management system and data analyzer.

Disk Storage

Currently, SSEC’s McIDAS has a storage capacity of approximately 33.8 gigabytes (33.8 billion bytes). The disk storage is divided into 6999 digital areas in which several databases reside. Three of the major databases are:

- image files
- Meteorological Data (MD) files
- grid files

An image (area) file contains digitized satellite visual or infrared sensor data. An MD file is a generic file for single location observations (nonimage). It accommodates many types of data under one general structure. A grid file contains fields analyzed at regularly-spaced latitude and longitude locations (grids) from observational data.
Non-video Terminals and Cluster Controller

Non-video terminals are used for ongoing development of system software. The Cluster Controller is an interface between the non-video terminals and the IBM mainframe computer.

Local Area Networks

SSEC’s McIDAS supports three Local Area Networks (LANs). Two LANs function as operational networks while the third is used for workstation development and testing. The LANs are high speed data links between the McIDAS workstations and the IBM computer. McIDAS uses two off-the-shelf LANs, ProNET and Ethernet.

ProNET is a proprietary LAN manufactured by Proteon, Inc. The LAN is a two-card set. One card plugs into an adapter slot in the PS/2; the other card plugs into a Multisourcerer. The Multisourcerer is an interface between an IBM I/O channel and the ProNET card installed in the Multisourcerer. This card links up to 15 McIDAS workstations to the Multisourcerer. ProNET transfers data serially at a rate of 10 megabits per second.

Ethernet is a LAN developed by the Xerox, Digital Equipment (DEC) and Intel Corporations. In McIDAS, it links workstations to an IBM computer’s I/O channel via the Interconnect Controller (IBM 3172). Ethernet transfers data serially at 10 megabits per second.

Remote Communications Controller

The Remote Communications Controller is an interface between the IBM computer and:

- remote workstations (dial-up)
- other McIDAS installations
- conventional meteorological data inputs
- weather radar inputs

The Remote Communications Controller links asynchronous dial-up workstations to the IBM computer. The characteristics of these workstations are similar to the Bisync link described above.

The Remote Communications Controller allows SSEC’s McIDAS to exchange a variety of conventional weather data with other McIDAS CPUs. This conventional data, called point source data, is used to maintain the Meteorological (MD) database. Sources for conventional data include radiosondes, rocketsondes, ship reports, aircraft and radar.
Overview

Tape Controller and Tape Drives

The McIDAS operating system is stored on magnetic tape. The Tape Controller selects and controls the appropriate Tape Drive. Modifications to the McIDAS operating system, such as those resulting from ongoing development, are output to a Tape Drive. During initialization, the operating system is loaded into the IBM computer via the selected Tape Drive and Tape Controller.

McIDAS Workstation

The McIDAS workstation, which is designed for animated display of satellite imagery and weather data, has the following features:

- real-time access to image and conventional data
- graphics overlays of images without image destruction
- animated displays of image or graphics frames at user selectable looping rates up to 15 frames/second
- pseudocoloring of imagery
- user selected graphics colors
- manual graphics drawing using the mouse
- satellite image combinations, forming 3-dimensional color enhanced images
McIDAS WWW Description

Figure 2 on the next page shows the components that make up a complete WIDE WORD Workstation. Blocks containing an asterisk (*) may be omitted in some workstations, with a corresponding reduction in workstation capability and flexibility.

The line in Figure 2 that connects the IBM PS/2 to the IBM host is shown as a direct connection. More precisely, this line may consist of a ProNET or Ethernet LAN, or an asynchronous link via the Communications Controller and Protocol Converter. Regardless of the link type, there is a bidirectional data path between the IBM host and the IBM PS/2. All blocks in Figure 2, with the exception of the IBM host block, make up a WWW.

IBM PS/2 Model 70 or 80 System

The IBM PS/2 system provides the workstation intelligence and contains the following components:

- IBM PS/2 Model 70 or 80 (20 or 25 MHz) computer
- keyboard
- mouse
- WIDE WORD PS/2 Interface
- ProNET or Ethernet Adapter
- Dual Asynchronous Adapter
- color monitor (Zenith Model ZCM-1492 or equivalent)

Each of these components is described below.

IBM PS/2 Computer

Most WWW installations are based on the IBM PS/2 Model 70. The main difference between the Model 70 and 80 is the number of card adapter slots. The Model 70 has three adapter slots; the Model 80 has eight. Typically, the PS/2 to WIDE WORD Workstation Interface, the ProNET Adapter and the Dual Asynchronous Adapter cards are installed in the Model 70's three slots. This provides the Model 70 with three asynchronous ports (the Model 70 has one built-in asynchronous port), one parallel port, LAN capability and an interface with the Dataram WIDE WORD Chassis.
Figure 2. McIDAS WWW System Configuration
Regardless of the PS/2 model used, the clock frequency should not be less than 20 MHz. Also, the PS/2 must have a minimum of 8M bytes of memory. This is accomplished by inserting memory modules in the PS/2. The PS/2 integrates the keyboard, mouse and color monitor into a user interactive terminal. The PS/2 relieves the host of some of its workload by performing many of the workstation related tasks at the workstation. This is in contrast to some of the older style non-PC based workstations.

Keyboard

The keyboard is a standard keyboard supplied with the IBM PS/2 computer. The user interacts with McIDAS via the PS/2's keyboard to perform the following:

- request image and/or graphics frames from the host
- establish display loops
- create and modify graphics frames
- erase portions of or an entire graphics frame
- select zoom factors
- roam within an image
- position one or both cursors
- define the size and shape of the cursors
- display stereo images
- colorize images
- define graphics colors
- label displays
- display multiple image and/or graphics frames simultaneously by partitioning the display
- perform high and low level diagnostics
- blink portions of the display
- read back from the Dataram

The keyboard is documented by its manufacturer.
Overview

Mouse
The mouse provides the PS/2 with cursor control. It is used with the roam feature and for cursor (flashing underline symbol) positioning during alphanumeric displays on the color monitor.

WIDE WORD PS/2 Interface
The WIDE WORD PS/2 Interface is an IBM PS/2 compatible printed circuit board designed and built by SSEC. It links the address, data and control signals in the PS/2 to SSEC's B Board in the Dataram WIDE WORD Chassis. This card makes all addressable sections in the Dataram WIDE WORD Chassis appear as memory and I/O extensions of the PS/2.

ProNET or Ethernet Adapter
When several workstations are located within a few hundred feet of the host, they are usually connected to the host via a Local Area Network (LAN). McIDAS uses ProNET and/or Ethernet LANs. These LANs are circulating token ring types and require an access adapter for each ring (workstation or host) member.

The host's adapter resides in a Multisourcerer. The Multisourcerer links the LAN adapter to the IBM channel. The workstation's adapter resides in the PS/2. The LAN allows the workstations to communicate with the host at a 10M bit/second rate. However, the total throughput is less than 10M bit/second because of the IBM channel speed and time required for buffer loading.

Dual Asynchronous Adapter
The Dual Asynchronous Adapter expands the number of asynchronous communications ports from one to three. This allows the use of a serial printer on one port, a modem on another (when a workstation is remoted via a modem to the McIDAS host) and a spare.

Color Monitor
Currently, the WWW uses a 14" Zenith Model ZCM-1492 color monitor. This RGB (Red, Green, Blue) monitor connects directly to the PS/2 computer. The monitor requires 0.7V RMS red, green and blue drive signals, and horizontal and vertical sync from the PS/2. The monitor is non-interlaced and has horizontal and vertical scan frequencies of 31.5 KHz and 60 Hz, respectively. Other monitors meeting these specifications may be substituted.
Dataram WIDE WORD Chassis

The Dataram WIDE WORD Chassis consists of an off-the-shelf memory storage system produced by Dataram Corporation and two custom SSEC designed boards built on Dataram form factor boards. These SSEC boards are called WIDE WORD McIDAS Board A and Board B (hereafter referred to as A Board and B Board, respectively). The memory storage system stores image and graphics frames requested from the host by the user. The A and B Boards, under control of the PS/2, convert the requested frames into RGB monitor signals.

Memory System

The term WIDE WORD comes from the length of the data words. This memory system stores and retrieves 128-bit data words. A typical non-McIDAS WIDE WORD Chassis configuration consists of:

- 1 to 16 dynamic RAM array memory boards (must be installed in sets of 4, 8, 12 or 16 boards for workstation applications)
- two data bus management boards
- a system control board
- one or more interface boards (seven maximum)

In the WWW configuration, the standard interface cards are replaced by the A and B Boards. Thus, from Dataram's perspective, these cards are interface cards. All SSEC customized electronics, with the exception of the WIDE WORD PS/2 Interface, reside on the A and B Boards.

Frame Storage Requirements

A McIDAS TV frame is defined as 480 horizontal lines of 640 pixels each. In the WWW, each pixel is represented by 8 bits. Since each WIDE WORD contains 128 bits, they each represent 16 pixels \(16 \times 8 = 128\). A full resolution WWW horizontal line consists of 40 WIDE WORDs \((40 \text{ words} \times 16 \text{ pixels} = 640 \text{ pixels})\). Therefore, a full resolution TV frame consists of 19,200 WIDE WORDs, \((40 \text{ words/line} \times 480 \text{ lines} = 19,200 \text{ words})\). This is the minimum storage requirement for each stored image or graphics frame.

Memory Partitioning

The WWW memory space, unlike the older tower system, is not segmented as explicit frames but is continuous memory space. This means that users are not restricted to 640 x 480-sized frames. In principal, the entire memory space can be used as an M pixel by N line dimensioned frame. Frames larger that the standard TV frame \((640 \times 480)\) are called "super frames."
The memory is arbitrarily partitioned as M by N arrays of image or graphics frame space. The ratio of image frames to graphics frames is arbitrary; it was fixed at 2:1 in the tower workstation. A frame is implicitly specified by a start location (the upper left corner), the line length M, and the number of lines N. Thus, the storage memory can be partitioned into a mixture of TV and super image and graphics frames. Depending on the number of array memory boards installed in the chassis and the type of chips installed in the array memory boards, the WWW can store 27 to 1799 TV frames (8 to 512M bytes).

The WIDE WORD A Board performs all TV display functions. Specifically, it:

- converts the requested frame(s) stored in the memory as 128-bit digital words to horizontal scan lines of analog video
- produces all necessary WIDE WORD clocking signals and the TV timing signals (horizontal and vertical sync plus blanking) required for displaying TV images
- generates the cursors and image labels
- colorizes the images
- blinks requested portions of the display
- processes images simultaneously through two identical yet separate image channels called Image Channel 1 and Image Channel 2
- drives a third channel, called the Dual Channel, with either image channel or both image channels simultaneously
- contains a graphics channel that can be multiplexed onto any of the three image channels

The WIDE WORD workstation outputs non-interlaced Image Channel 1, Image Channel 2 and Dual Channel video to its rear panel. The Dual Channel output is the standard output because it can display any of the individual channels plus combinations of channels. Within the A Board, the Dual Channel drives an interlace converter that produces an interlaced RGB output for driving an optional NTSC (National Television Standards Committee) Encoder. The NTSC Encoder produces a composite NTSC output for use in TV studios, etc., and driving the optional NTSC monitor.
If the A Board is equipped with the optional WIDE WORD Interlace Adapter Board (daughter board that is plugged onto the A Board), Image Channel 1 and Image Channel 2 are converted to interlaced format in the same manner as the Dual Channel. However, these channels are no longer available at the rear of the WIDE WORD chassis in the non-interlaced format. These channels can still be displayed in the non-interlaced format via the Dual Channel output.

The WIDE WORD B Board is the interface between the PS/2, Dataram and A Board. From the PS/2's perspective, the Dataram memory, A Board and B Board appear as memory and I/O ports. This board contains two interface sections: the PS/2 to Dataram Interface and the PS/2 to A Board Interface.

The PS/2 to Dataram Interface allows the PS/2 to:

- store an image or graphics frame
- read an image or graphics frame
- erase all or part of an image or graphics frame
- modify a graphics frame at the bit, byte or word level

The PS/2 to A Board Interface allows the PS/2 to:

- set the zoom factor
- set the cursors' size, position and type
- program the frame label memory
- set the display mode, e.g., full screen, horizontal or vertical split screen or quad panel
- disable the cursor(s) or labels and blank portions of the display
- enable or disable graphics bit planes
- load colorizer tables
- set the blink rate and/or enable/disable blinking
- construct nonstandard cursor shapes
- roam within a selected image
WWW Functional Description

The WWW is a collection of commercial and custom electronic devices. Documentation for the commercial devices is furnished by their respective manufacturers and is not repeated here. The WIDE WORD PS/2 Interface and the A and B Boards are documented in detail in this manual. The documentation consists of a Simplified Functional Description, Detailed Functional Description and Detailed Circuit Description for each card (the WIDE WORD PS/2 Interface card contains only one functional level).

It would be difficult, if not impossible, to understand these boards from a functional or circuit perspective without at least a cursory understanding of the commercial devices directly linked to the SSEC custom boards. Specifically, you need to know about the PS/2 architecture to understand the WIDE WORD PS/2 Interface. You also need to know about Dataram characteristics to understand the A and B Boards. Therefore, the PS/2 architecture and Dataram WIDE WORD characteristics are presented below. For additional information, consult the manufacturer's documentation.

PS/2 Architecture

The PS/2 connects to the WIDE WORD chassis via the WIDE WORD PS/2 Interface card, which is a printed circuit card developed by SSEC that plugs into the PS/2's Micro Channel™.

PS/2 Hardware Sections The PS/2 Model 70 or 80 computer has a number of hardware blocks that are interconnected by the microprocessor's address, data and control lines. Collectively, these lines are called the Micro Channel. Each hardware block is assigned a unique block of memory and/or I/O address space. The PS/2 hardware blocks are:

- ROM (Read Only Memory)
- DMA (Direct Memory Access)
- Math Coprocessor (optional)
- RAM (Random Access Memory)
- Diskette Control
- Video Graphics Control

* Micro Channel is a trademark of IBM.
- RS-232 Serial Port
- Parallel Port
- Interrupt Controller
- Timer (Three Channels)
- Keyboard and Mouse Control
- Clock/Calendar
- Spare Micro Channel Connectors

Micro Channel Characteristics

The PS/2 uses an Intel 80386 32-bit microprocessor. For backward compatibility with less powerful microprocessors, the 80386 can operate with 8-, 16-, 24- or 32-bit data words (1-4 bytes). Further, the 80386 can transfer data to or from other devices over a 16- or 32-bit wide data bus. Bus width control is accomplished via an input pin that is controlled by the memory or I/O mapped hardware block being addressed (i.e., WIDE WORD PS/2 Interface card).

The data bus component of the Micro Channel is 32 bits wide for maximum internal data throughput. However, devices connected to the Micro Channel may be either 16-bit (such as the WIDE WORD PS/2 Interface) or 32-bit devices. When a data word longer than 16 bits is transferred to or from a 16-bit device, the 80386 performs multiple bus cycles.

The 80386 has 30 address output lines (A2-A31) and four byte enable lines (BE0-BE3). BE0-3 are generated by internally decoding A0 and A1. BE0-3 identify the active bytes on the 32-bit Micro Channel. A0 and A1 are reconstructed external to the 80386 and are part of the Micro Channel's address signals. Thus, the Micro Channel's address bus is 32 bits wide (A0-A31). BE0-3 are also part of the Micro Channel's control signals.

For added flexibility and memory utilization, two additional features are provided. First, multiple byte operands may be split between two physical words in the memory array. For example, two 16-bit and four 8-bit operands (8 bytes total) can be stored in two physical words (8 byte capacity) in the memory array. Thus, an operand can start with any byte within the physical word provided all bytes in the multiple byte operand are contiguous. The 24- and 32-bit modes are not used in the workstation application. Second, operands or portions of operands that reside only in the upper half of a 32-bit physical word are duplicated on the lower 16 bits of the Micro Channel's data bus. This results in a higher data throughput when the Micro Channel is forced into the 16-bit mode because data does not have to be translated to the lower half of the bus by the slave device.
## 80386 Data Lines

<table>
<thead>
<tr>
<th>(Upper Bus)</th>
<th>(Lower Bus)</th>
<th>16-Bit Micro Channel Bus Signals</th>
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<tbody>
<tr>
<td>Byte 4</td>
<td>Byte 3</td>
<td></td>
</tr>
<tr>
<td>D31-24</td>
<td>D23-16</td>
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**S**

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<th>Comments</th>
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<tbody>
<tr>
<td>Double Bus Cycle: Byte 2, then Byte 3</td>
</tr>
<tr>
<td>Double Bus Cycle: Bytes 1-2, then Byte 3</td>
</tr>
<tr>
<td>Double Bus Cycle: Byte 2, then bytes 3-4</td>
</tr>
<tr>
<td>Double Bus Cycle: Bytes 1-2 then 3-4</td>
</tr>
</tbody>
</table>

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S = active byte in single-byte operands  
D = active bytes in double-byte operands  
T = active bytes in triple-byte operands  
Q = active bytes in quadruple-byte operands  

* BHE is asserted (active) when zero (0)

---

**Table 1. Micro Channel Data Transfers**
Table 1 on the adjacent page shows each valid operand location within a physical word. Byte High Enable (BHE) is a Micro Channel signal that, together with A0 and A1, describes which data bytes are read from or written to the Micro Channel device while in the 16-bit mode. When operands extend across the upper/lower bus boundary, the 80386 sends or receives the active lower bus portion first. Then it performs an additional bus cycle to send or receive the upper bus portion.

As an example of the multiple bus cycle concept, consider the first triple-byte operand in Table 1. The BHE, A1 and A0 code (0, 0 and 0) is the same as the code for the first double-byte and the quadruple-byte operands. The code is the same because both lower bus bytes are active for each operand. That is, the code shown for each double bus cycle operand is the code for the first cycle. Once the first bus cycle is completed, a second bus cycle is executed if the operand transfer is not complete. In the triple-byte operand, the BHE, A1 and A0 for the second bus cycle are 1, 1 and 0, respectively. Note in Table 1 that this code is the same as the code for a single-byte operand located on the 80386’s D16-D23 data lines.
Figure 3. DR-429 Memory System
Dataram WIDE WORD System Characteristics

The Dataram Corporation’s System 2000F consists of a 19-inch rack-mountable chassis containing a DR-429 Memory System and seven interface card slots. In a typical system, the interface card slots contain one to seven interface boards that interface the WIDE WORD memory to one or more CPUs. In the MCDAS WWW, SSEC’s A and B Boards are inserted in two of the interface slots. These boards not only interface the DR-429 Memory System to the PS/2, but also provide all the workstation’s display functions.

Memory System Components

Refer to Figure 3 on the adjacent page. The DR-429 Memory System consists of:

- from 1 to 16 WIDE WORD Semiconductor Array (WSA) boards
- two WIDE WORD Semiconductor Data (WSD0-1) boards
- a WIDE WORD Semiconductor Control (WSC) board

In SSEC’s WWW, WSA boards must be installed in sets of four cards, i.e., 4, 8, 12 or 16.

WSA Characteristics

The WSA cards are Dynamic Random Access Memory (DRAM) storage arrays. The WSA board has both a 160-bit and 128-bit data word version. The 128-bit data word version actually contains 144 bits. The extra 16 bits in each word store an Error Correction Code (ECC). In addition, each version can be populated with 64K, 256K or 1M DRAMs. The WWW uses the 128-bit data word version and normally uses 256K bit DRAMs. Since the WWW requires WSA boards in sets of four, each WSA board set provides 32M bytes of storage.

WSD Characteristics

The WSD boards manage the 128-bit data bus and perform error correction. The DR-429 Memory System’s data bus consists of two 64-bit buses. WSD0 manages the lower 64-bit bus; WSD1 manages the upper 64-bit bus. Each 64-bit word has its own 8-bit ECC. Thus, there is a total of 128 bits plus 16 ECC bits. When data is stored, the respective WSD boards calculate an ECC based on its 64 data bits. The ECC is stored with the word.

During data retrieval, the respective WSD board computes a new ECC based on its retrieved 64 bits and compares this code with the previously stored code. If there is a single bit error in one or both 64-bit words, the error is automatically corrected by the respective WSD card. If there is more than one error in a 64-bit word, the errors are detectable, but uncorrectable. Thus, depending on the error bit distribution, up to two errors can be corrected in a 128-bit word (one bit in each 64-bit word).
If the WSD boards detect an error, a logging message is assembled and sent to the WSC card for storage (logging). The message identifies the bit failure to a specific chip on one of the WSA cards. Refer to the WSC Characteristics information below and the Switches and Indicators description on page 1-22 for additional information on error logging.

WD000N-WD790N (WIDE WORD data bits 0-79, lower bus word) are the WSD0 input data bus lines; WD001N-WD791N (WIDE WORD data bits 0-79, upper bus word) are the WSD1 input data bus lines. These bus lines link the WSD boards to the A and B Boards via the Dataram’s back plane. AD000N-AD790N are WSD0’s bus lines to and from the WSA boards; AD001N-AD791N are WSD1’s bus lines to and from the WSA boards.

WSC Characteristics

The WSC board contains the logic to control up to 16 WSA boards. The WSC board performs the following functions:

- address storage and control (maps addresses into row, column and WSA board enable signals)
- system timing and control
- error logging, storage and control
- battery backup control
- refresh timing and control
- bus priority control

System Interconnections

Figure 3 on page 1-18 shows the major signal lines that link the WSC board to the WSA card. These signals and their functions are:

- AAR00N-AAR19N (Array Address lines 00-19)
- ABDS0-ABDS3 (Array Board Select -- selects one of 16 WSA boards)
- ABTHDN (Array Battery Hold -- described below)
- AODA0-AODB1 (Array Output Data Enables -- enables the data output of selected WSA boards)
- ARSA0-ARSB3 (Array Row Address Strobes A0-A3 and B0-B3)
- AWRA0N-AWRB3N (Array Write Strobes A0-A3 and B0-B3)
The DR-429 Memory System can be equipped with an optional battery backup unit that plugs into an external rear panel 6-pin connector located just above the AC power cable. It prevents the memory from losing data during a power disruption. The battery backup unit is a Dataram model BA-102. It is described in Dataram Product specification P/N 02223.

At the present time, no battery backups have been requested or provided. However, this option could be installed if the need arises. When so equipped, ABTHDN is used during battery backup operation.

Refer to Figure 3. In addition to mating with the Dataram backplane via the interface card slot connectors (four 96-pin connectors), the A and B cards are connected to each other with two 50-conductor ribbon cables (JA and JB). These cables pass address, data, control and timing signals from one board to the other.

In simplest terms, the A Board reads from the Dataram and the B Board writes to the Dataram. In addition, the B Board can read from the Dataram for the purpose of graphics modification by the user. Thus, the B Board has a read/write capability, while the A Board has only a read capability. Since both boards access the Dataram, they require a separate Dataram interface. That is why both cards link Handshake, Address and Control to the WSC boards, and each card links data signals to the WSD Board.

The A Board has a connector labeled VP (Video Port). It is a 20-line coax ribbon cable (75 ohm) that carries the workstation’s monitor drive outputs. These signals consist of RGB drive and Sync for Image Channel 1, Image Channel 2, Dual Channel and NTSC. The B Board has a connector labeled JC that connects to the PS/2 computer. It carries address, data and control signals.
Dataram Controls and Modes of Operation

Switches and Indicators  The Dataram System 2000F cabinet contains these three front panel switches:

- AC ON/OFF
- Error log clear/begin (CLR/BGN)
- Error log examine (EXM)

It also has five LED indicators:

- LOG FULL
- Error (ERR)
- Ready (RDY)
- Board, Row, Bit, Word (BOARD, ROW, BIT, WORD) 6-digit display
- Fan Failure LED

All switches and indicators, except the Fan Failure LED, are located in the chassis' lower-right front panel. With the exception of the AC ON/OFF switch, Fan Failure and RDY LEDs, all switches and indicators are part of an error logging display system. The RDY LED illuminates after a successful power-up sequence.

Error Log Interpretation  As previously described, the WSDs provide a logging message to the WSC board in the event of an ECC failure. The front panel switches and indicators allow the contents of the WSC log to be read directly from the front panel display. The log has a 16-word capacity. The contents of each log address can be viewed on the 6-digit display. The remaining front panel switches and indicators control the display and log.

The CLR/BGN switch is a spring loaded three-position toggle switch (center is off). Moving this switch to the CLR (up) position clears the log. The log is also cleared during power-up. Move this switch to the CLR position only after recording errors. Moving this switch to the BGN (down) position resets the log display address to zero, but does not clear the log. If one or more errors occur, the ERR LED will light and remain lit until the log is cleared. If the ERR LED lights, toggle the CLR/BGN switch to the BGN position and view the first error message by toggling the EXM (examine) switch. This switch is a spring loaded, two-position toggle switch that is normally off. It must be pressed to examine a log entry. If 16 or more errors are detected, the LOG FULL LED lights and no additional errors are recorded.
The 6-digit LED display describes failures to the chip level. An example of a log display is:

```
  15  1  64  1
 BOARD ROW BIT WORD
```

The 15 indicates the failure is on board WSA15. If your maintenance policy is board replacement, record the error message and include it with the defective board when returning it to SSEC or Dataram Corporation. If your maintenance policy is component replacement, you must decode the remaining four digits of the error message to locate the defective chip.

The WSA printed circuit board is used in two WIDE WORD chassis, the DR-429 (used in the WWW) and a DR-329. In both versions, the WSA card contains 288 DRAMs arranged physically in eight rows of 36. Electrically, the chips on the DR-429 configuration are arranged as two rows of 144 chips; the chips on the DR-329 are electrically arranged as four rows of 80 chips (72 for ECC versions). The silk screened row information on the WSA card applies to the DR-329. Therefore, the ROW information in the error message, the second digit in the display, does not correspond to the row information silk screened on the card. The ROW information in the error message is the electrical row numbered 0-1. This number must be mapped to a physical row to locate the bad chip. This is done with the aid of the ROW, BIT and WORD digits in the message.

To locate the defective chip, turn off the AC power, open the cabinet, remove the defective WSA board and place it on a flat surface with the component side up and the top of the board pointing away from you. Directly below the upper eight rows of chips you will see a silk screen matrix with numbers ranging from 000-791. A separate silk screen column in this matrix corresponds to each column of DRAMs. However, each matrix block represents two physical row chips within its column. Match the three right-hand digits in the displayed error message to the three corresponding matrix digits (641 in the above error message example). This identifies the matrix block where the defective chip lies, and reduces the number of chip possibilities to two.

Next, identify the physical row. Each block in the matrix contains a ROW0 chip and a ROW1 chip. The ROW0 chip is the lower (closest to you) of the two chips. The error message's electrical ROW readout, 0 or 1, indicates the lower and upper chip, respectively, in a matrix block. In the above example, the ROW digit is 1, indicating the upper chip in the 641 matrix block.
Data Transfer Modes

The Dataram WIDE WORD Memory System stores 128-bit words. The Memory System can read or write in word lengths from 1 to 16 bytes using these six primary modes of operation:

- **WIDE WORD Read** -- reads a 128-bit word from the memory location specified by the address bus.
- **WIDE WORD Write** -- writes a 128-bit word to the memory location specified by the address bus.
- **Write Byte** -- stores one to nine bytes in the memory location specified by the address bus.
- **Read-Modify-Write (RMW) Byte** -- modifies one or more of the 16 bytes in the addressed location.
- **Read-Modify-Write (RMW) WIDE WORD** -- modifies any bit or bits in the WIDE WORD specified by the address bus.
- **Sequential Read or Write** (described below).

In all but the Sequential modes, the external CPU (or in the case of the WWW, the A or B Board) provides an address each time a read or write cycle is initiated. When multiple sequential addresses are read from or written to, a sequential read or write mode can be used. In these modes, only WIDE WORDs may be read or written. Only an initial address is sent to the WSC card. Thereafter, all addressing is performed locally by the WSC card. The cycle begins with a 400 nsec Sequential Synchronization phase, followed by a variable length Sequential Read or Write phase, and terminated with a 400 nsec Sequential Halt phase.

During the Sequential Synchronization phase, the WSC card latches the starting address and monitors the read/write status lines and the ascending/descending address status line to determine at what address the cycle begins, whether it is the lowest or highest address for the cycle and whether it is a read or write cycle.

The Sequential Read or Write phase retrieves or writes WIDE WORDs until it is terminated by a Sequential Halt phase. The Sequential Read or Write phase varies in length depending on the number of words stored or read. Each read or write cycle requires a minimum of 100 nsec.

While the Sequential Mode has a fixed overhead of 800 nsec (synchronization time plus halt times), the Read or Write phase of this cycle is a minimum of four times faster than any of the other primary modes described above. This is an ideal mode for the A Board since it reads images that have been stored as a sequence of WIDE WORDs.
The six primary modes result in 84 unique memory read/write modes that are specified by four mode control lines and ten byte select/word length control lines. The Byte Write primary mode, with its 38 variations, isn't used in the WWW. The Read-Modify-Write Byte mode consists of 16 read/write modes. The only difference between these modes is a byte select code. The Sequential Write Mode is not used and the remaining primary modes have no variations. Thus, only 20 of the 84 memory read/write modes are used with the the WWW. The modes used in the WWW are:

- Sequential Read -- A Board
- WIDE WORD Read -- B Board
- WIDE WORD Write -- B Board
- Read-Modify-Write Byte -- B Board (16 unique read/write cycles)
- Read-Modify-Write WIDE WORD -- B Board

The Dataram WIDE WORD Memory System uses these four interlocked handshake signals to control the storage and retrieval of data:

- WADAVN (WIDE WORD Address Available)
- WADACN (WIDE WORD Address Acknowledge)
- WDTRQN (WIDE WORD Data Request)
- WDTACN (WIDE WORD Data Acknowledge)

A storage or retrieval cycle begins when the A or B card asserts WADAV/(labeled WADAVN in the Dataram). WADAVN must remain asserted until the WSC Board responds with WADACN (labeled WADAC/ in the A and B Boards). When the A or B card recognizes the WADACN signals, it removes the WADAVN signal. When WSC recognizes the loss of the WADAVN signal, it removes the WADACN signal. Now, the memory is ready to read data from or write data to the address that it just accepted.
If this is a data read cycle, the A or B Board asserts WDTRQN. Upon recognizing the data request signal, the memory fetches the data from the previously accepted address location, places it on the data bus and asserts WDTACN. WDTACN informs the A or B Board that its requested data is available. When the data acknowledge is asserted, the A or B Board latches the data and cancels the data request signal. Upon cancellation of the data request, the WSC board cancels the data acknowledge signal, completing the cycle. If this is a Sequential Read cycle, WDTRQN may now be reasserted. That is, the address transmission process is not repeated.

In a data write process, the A or B Board places the data on the memory's data bus and asserts WDTRQN. The memory stores the data at the address specified and asserts WDTACN to inform the A or B Board that its data has been stored. Upon detecting the WDTACN, the A or B Board cancels its WDTRQN signal.

**Refresh Requirements**

Refresh cycles prevent data loss in the MOS DRAMs. The DRAMs are refreshed by strobing their row lines. Each DRAM must have all row lines strobed at least once every 2, 4 or 8 milliseconds for the 64K, 256K or 1M DRAMs, respectively.

The Dataram WIDE WORD Memory System can be configured for internal or external refresh. Internal refresh is performed entirely by the Memory System, but may cause delays up to 1.4 msec, depending on the mode of operation. This method of refresh is unacceptable for the WWW application since up to 120 WIDE WORDs must be read every 31 usec (three channels of video at 40 WIDE WORDs/channel). Consequently, the external refresh was selected for the WWW. The A Board generates all refresh enable gates. The refresh gates are generated so that all refresh occurs during horizontal blanking time. For more information on refresh timing, refer to the Raster Read Timing documentation in the A Board chapters of this manual.

For additional information on the Dataram WIDE WORD Memory System, refer to the technical manual DR-329/429 WIDE WORD 64K/256K/1M Memory System (P/N 06238, Rev A) and the WIDE WORD System 2000F Technical Manual (P/N 06245, Rev A). These manuals are available from Dataram Corporation and should have been provided when your workstation was delivered.
# PS/2 Interface Functional Description

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PS/2 Interface Functional Description

The WIDE WORD PS/2 Interface card plugs into a card adapter slot in the PS/2. The adapter slots are connected to the PS/2's Micro Channel. Some Micro Channel signals are not available at the Micro Channel connectors. Some signals available at the connectors are not required by the interface card or the WIDE WORD chassis. For complete Micro Channel specifications, refer to the IBM Personal System/2™ Model 80 Technical Reference.

The WIDE WORD PS/2 Interface Functional Block Diagram is shown in Figure 4 on the next page. It consists of these blocks:

- Memory Address Decode and Interrupt Logic
- Address Latch and I/O Decode
- Data Bus Transceivers
- Channel Control Logic

Memory Address Decode and Interrupt Logic

Each device in the Micro Channel responds to a unique group of memory and/or I/O addresses. The interface card has a memory block and an I/O block assigned to it.

The Micro Channel contains 32 address lines labeled A0-A31, resulting in a 4 gigabyte addressing range. The control signal MADE is the Micro Channel adapter enable signal. It is asserted during memory read or write cycles when the levels on address lines A24-A31 are low. Thus, MADE is asserted for addresses 00000000H-00FFFFFFH. The least significant 24 address lines (A0-A23) are wired to the Micro Channel connectors, resulting in a 16 megabyte addressing range. Of these lines, the upper seven (A17-A23) are used as a board address decode. This leaves address lines A0-A16 as usable address lines, resulting in an address range of 128K bytes.
Figure 4. WIDE WORD PS/2 Interface Functional Block Diagram
The Memory Address Decode and Interrupt Logic block, using MADE as an enable, outputs a control signal to the Channel Control Logic block for Micro Channel addresses C00000H-C1FFFFH.

The Memory Address Decode and Interrupt Logic block drives Interrupt Request line 15 (IRQ15) on the Micro Channel in response to an output from the Noise Gate block. The Noise Gate block is driven by FRAME INT (Frame Interrupt) which is asserted for a short time (about 1.3 msec) at the beginning of each display frame. The frame rate is about 30 frames/second. The Noise Gate opens, allowing FRAME INT to pass to the Memory Address Decode and Interrupt Logic block just before the expected arrival of FRAME INT.

When FRAME INT arrives, the gate closes until just prior to the next expected FRAME INT. This reduces the possibility of any noise on the FRAME INT input line causing false interrupts. The PS/2 uses the interrupt to determine when the various ports, registers and memories on the A Board require updating. Once IRQ15 is asserted, it remains asserted until either the PS/2 is reset or the PS/2 reads I/O port 334H which functions as an interrupt acknowledge.

**Address Latch and I/O Decode**

The Address Latch and I/O Decode block latches the 17 LSB Micro Channel address lines (A0-A16) on the rising edge of ADL (Address Latch). It also outputs a signal to the Channel Control Logic block when the Micro Channel is in an I/O cycle and the address on the 16 LSBs of the address bus is in the range 0334H-033FH.

**Data Bus Transceivers**

The Data Bus Transceivers pass data between the WIDE WORD chassis and the Micro Channel. Data direction is controlled by the Channel Control Logic.
Channel Control Logic

The Channel Control Logic links the Micro Channel’s control lines to the WIDE WORD chassis control lines. Each WIDE WORD control signal is described below, followed by the remaining Micro Channel signals.

IOR, IOW, MR and MW (I/O Read, I/O Write, Memory Read and Memory Write, respectively) are formed from CMD, S0, S1 and MIO (Command, Status bits 0 and 1, and Memory Input Output, respectively). CMD acts as an enable. Read or write data is always valid when CMD goes from active (low) to inactive. S0 and S1 are status bits that distinguish between read and write cycles. MIO distinguishes between memory and I/O cycles. MIO is high during memory cycles and low during I/O cycles. Table 2 below summarizes these control signals.

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<tr>
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<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
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</table>

Table 2. Channel Control Summary

RESET is produced by inverting CHRESET (Channel Reset). CHRESET is generated by the PS/2 to reset or initialize all adapters during power-up. This signal can also be asserted under program control. CHRESET is also used by the IRQ15 logic which is described on page 2-3.

Interrupt Reset (INT RESET) is asserted during a PS/2 reset or when the PS/2 reads I/O port 334H. This signal clears the Frame Interval interrupt latch portion of the Memory Address Decode and Interrupt Logic block. This signal is formed from:

- CHRESET
- S0
- S1
- MIO
- A1-A3
These signals, except for CHRESET, are required to recognize a port 334H read cycle.

Channel Ready (CHRDY) is normally asserted. It is used by channel slaves to extend read or write cycles up to 3.5 usec. It forces the PS/2's microprocessor into wait states until it goes active again.

Card Selected Feedback (FEEDBACK) is an acknowledge to the Micro Channel that a memory or I/O read or write cycle directed to the card's memory or I/O space was recognized. This signal is generated from acknowledge signal outputs of the Address Latch and I/O Decode, and the Memory Address Decode and Interrupt Logic blocks.

SELECT 16 is formed in the same manner as FEEDBACK. This signal forces the 80386 microprocessor into the 16-bit data mode whenever it reads or writes to the WIDE WORD chassis.
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PS/2 Detailed Circuit Description

The schematic diagrams of the WIDE WORD PS/2 Interface are shown on SSEC drawing 6450-0574 (Revision D, dated 10/19/89). This detailed circuit description discusses the logic of each block shown in the functional block diagram in Figure 4 on page 2-2. These blocks are:

- Memory Address Decode and Interrupt Logic
- Noise Gate
- Address Latch and I/O Decode
- Data Bus Transceivers
- Channel Control Logic

Refer to Figure 4 and the schematics as necessary.

Schematic Conventions

The WIDE WORD PS/2 Interface is built on a PS/2 Micro Channel printed circuit form factor board. The IC chips are labeled U1 through U7 as indicated on the schematic diagram, Figure 4 and the silk screening on the board. In the description that follows, ICs are referred to by their U designator.

Logic Conventions

Logic signals are indicated by all uppercase letters and numbers, e.g., MADE. A logic signal name ending with a trailing slash represents an active low signal, e.g., MIO/.

Several conventions that can describe the state of a logic signal are: true or false, high or low, one or zero, and active or inactive. In the following description, all logic states are described as high and low. This convention best describes the physical condition of a logic signal and is better suited for troubleshooting.

Frequently, a logic signal is "asserted." If a signal with a trailing slash is asserted, it is low. If a signal without a trailing slash is asserted, it is high. Thus, asserted means that a signal is in its active state.
Memory Address Decode and Interrupt Logic

The Memory Address Decode and Interrupt Logic block consists of PAL U1 which:

- generates an address acknowledge for addresses 00C00000H-00C1FFFFH
- drives the direction input of the Data Bus Transceivers
- latches the gated interrupt input from the Noise Gate (U7)
- clocks the address latch portion of the Address Latch and I/O Decode section.

U1 is a 16L8A PAL and is described by the C1 PAL equations located in the Reference section of this manual.

U1 uses A17-A23 and MADE to drive its pin 19. MADE is asserted when the upper eight bits (A24-A31) of the PS/2's Micro Channel are all low. When MADE is asserted and A17-A21 are low and A22-A23 are high, U1's pin 19 goes low. Thus, pin 19 goes low for Micro Channel addresses 00C00000H-00C1FFFFH. This output signal is passed to U2 and U4 where it acts as an enable signal.

U1's pin 18 drives the direction (DIR) input of the Data Bus Transceivers (U5 and U6). U1, functioning as a noninverting buffer, uses its pin 17 input to drive its pin 18 output. The purpose of this buffer is to delay the pin 18 signal by one propagation delay (about 25 nsec). This delay is needed to match the transmit/receive transitions on the Data Bus with the transitions of the direction control input to U5 and U6. For more information on U1's pin 17 input, refer to the Pin 23 Output Information on page 3-5.

U7, the Noise Gate, drives U1's pin 9 with a gated interrupt. U1's pin 9 is programmed as a set/reset latch. Pin 12 (IRQ15) is the output of this latch. The latch is set if pin 9 goes high (asserted) for at least 25 nsec and the PS/2 is not currently reading I/O port 334H. Once the latch is set, it remains set until it is reset by U2. When the PS/2 reads port 334H, U2 drives U1's pin 11 low, clearing the interrupt latch. U2 also drives U1's pin 11 low during a power-up sequence, insuring that the latch is in the reset state following a power-up.

The address latch portion of the Address Latch and I/O Decode section (U3 and U4) requires a clock to strobe the PS/2's address inputs into the address latches. Pin 1 on U3 and U4 is the clock input to these latches. U1 generates the clock strobe (pin 16 output) by inverting ADL/ (Address Latch).
Noise Gate

U7, a monostable multivibrator, is the Noise Gate. When U7 is triggered by the rising edge of the PCINT/input to pin 5, the normally low pin 6 goes high for a period of time determined by the time constant of C1 and an internal resistance between pins 9 and 11 (about 2K ohms). With the 27UF capacitor, the pulse width is about 25 msec. Although this time is not critical, it should not exceed 32 msec. An excessive pulse width will result in missing every other interrupt, causing an apparent system slow down. Timing Diagram 1 on the next page shows the Noise Gate's input and output timing.

U1 passes the output of U7 through an inverter and applies it and the output of U7 to a NAND gate. The result is a narrow pulse equal in duration to the propagation delay through the inverter (about 25 nsec). This pulse drives the tri-state enable input to the IRQ15/ driver.

Address Latch and I/O Decode

The Address Latch and I/O Decode section consists of two 22V10 PALs located at U3 and U4. They are described by the C3 and C4 PAL equations located in the Reference section of this manual. Both chips function as 9-bit latches. U3 latches SBHE (System Byte High Enable) and the lower byte of the Address Bus (A0-A7); U4 latches the upper 9 bits of the Address Bus (A8-A16). U3 drives its pin 14 low for addresses xx34H-xx3FH; U4 drives its pin 14 low for addresses 06xxH (x = don't care). U2 combines these outputs to generate an I/O acknowledge for I/O addresses 0334H-33FH. For more information, see the Channel Control Logic description on page 3-5.

Data Bus Transceivers

U5 and U6 are the Data Bus Transceivers. U6 drives D0-D7; U5 drives D8-D15. The direction input (pin 1) is driven by U1's pin 1.
Timing Diagram 1. Frame Interval Timing

*Internal PAL terms - see the PAL equations for WWC1.
Channel Control Logic

The Channel Control Logic consists of a 22V10 PAL located at U2. This chip is described by the C2 PAL equation located in the Reference section of this manual. U2 is described below in terms of its outputs.

Pin 14 Output
U2's pin 14 resets the IRQ15 flip-flop in U1. Pin 14 goes low when the PS/2 is reset or powered up, or when it reads I/O port 334H.

Pin 23 Output
U2's pin 23 output is a latched signal that goes low when reading memory or I/O ports assigned to the WWW (I/O ports 334H-33FH and memory addresses 00C00000H-00C1FFFFH). U2's pin 23 output drives the direction control of the Data Bus Transceivers (U5 and U6) via a buffer in U1. U1's pin 17 is this buffer's input; pin 18 is its output.

CDDS16/
CDDS16/ (Card Data Select 16) informs the PS/2 that the WIDE WORD Interface card uses a 16-bit data bus width. This signal goes low during memory reads from or writes to addresses 00C00000H-00C1FFFFH and I/O port reads from or writes to I/O ports 334H-33FH.

CDSFDBK/
CDSFDBK/ (Card Selected Feedback) is identical to CDDS16/ in its formation. This signal acknowledges memory and I/O read/write cycles directed to the WIDE WORD PS/2 Interface card.

CDCHRDY/
CDCHRDY/ (Card Channel Ready) allows slow and/or multiplexed access devices to operate with the high speed Micro Channel. Microprocessor instructions require an acknowledge signal to complete. A slow device or a device that is currently busy forces the microprocessor to wait until the device has read or fetched the requested data by asserting CDCHRDY/ only after the slow or busy device has completed the transfer. Regardless of the WIDE WORD source or destination, the Ready signal is transmitted onto the Micro Channel immediately upon receipt of the command. This is possible because the PS/2 transfers data to and from high speed FIFOs and latches (fully buffered inputs and outputs).

PCRST/
PCRST/ (Personal Computer Reset) resets the Dataram memory when CHRESET (Channel Reset) is asserted on the Micro Channel. This signal is asserted during power-up and soft reset sequences.
**PS/2 Detailed Circuit Description**

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</tr>
<tr>
<td>PCMEMR/</td>
<td>PCMEMR/ (Personal Computer Memory Read) is asserted when the microprocessor reads memory addresses 00C00000H-00C1FFFFH.</td>
</tr>
<tr>
<td>PCIOW/</td>
<td>PCIOW/ (Personal Computer I/O Write) is asserted when the microprocessor writes to I/O ports 334H-33FH.</td>
</tr>
<tr>
<td>PCIOR/</td>
<td>PCIOR/ (Personal Computer I/O Read) is asserted when the microprocessor reads I/O ports 334H-33FH.</td>
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A Board Functional Description

The WIDE WORD A Board contains the WWW display characteristics. It has the features of the older tower workstation plus many new features. Some of these features are not yet implemented in the host software. This A Board documentation treats all features as if they are already implemented since they can be demonstrated and tested with diagnostic software residing in the PS/2.

Frame Characteristics

Operating in the Sequential Read mode, the A Board reads WIDE WORDs from the Dataram WIDE WORD Memory System. Each displayed pixel is represented by one byte. Since each WIDE WORD consists of 128 bits (16 bytes), each WIDE WORD represents 16 pixels.

The A Board simultaneously generates three video channels. Two of these channels are image channels; the third is a graphics channel. Since a horizontal line consists of 640 visible pixels, up to 40 WIDE WORDs (41 WIDE WORDs when roaming) per channel must be read and processed for each channel (3 channels x 40 words/channel = 120 words). The actual number of WIDE WORDs per channel is a function of the zoom and roam features.

Image and graphics frames are defined by the user and stored in the Dataram memory as a string of consecutive WIDE WORDs. A standard frame has 480 horizontal rows (scans) of 640 pixels each. A superframe can be any size as long as it is larger than a standard frame and is modulo 16. Since each WIDE WORD contains 16 pixels, 40 WIDE WORDs make up each horizontal row, and 19,200 WIDE WORDs represent a standard frame (480 lines x 40 words/line).
Channel Formation

A frame can start anywhere in the Dataram memory. For example, assume that image frame 1 occupies addresses 0-19199D, image frame 2 occupies addresses 19200D-38399D, and graphics frame 1 occupies addresses 38400D-57599D. If these frames are selected for display, all three frames are displayed simultaneously. The following paragraphs explain how this happens.

First, remember that the A Board retrieves data from the memory via the Sequential Read mode. In this mode, a starting address is sent to the memory during the Sync phase. Then WIDE WORDs can be read using only the data request and acknowledge handshake signals.

If the WWW was limited to displaying only one frame at a time, only one starting address would need to be sent. Then, the 19,200 words would be read, the data would be processed into an analog video stream and the read process would be halted at the end of the frame with a Sequential Halt cycle. This scenario assumes that the Dataram handshake signals are manipulated in such a way as to reduce the Dataram readout rate to the image pixel display rate. Otherwise, it would read out data about six times faster than the data can be displayed.

To display three frames simultaneously, a horizontal line of image 1 must be fetched and stored in a buffer; a horizontal line of image 2 must be fetched and stored in another buffer; a horizontal line of the graphics frame must be fetched and stored in a third buffer. Then all three buffers can be unloaded simultaneously at the pixel clock rate.

The output of each buffer is a separate channel. Thus, there are three parallel channels in the WWW. These channels can simultaneously process their respective buffer’s WIDE WORDs one byte (pixel) at a time. While the data for the current horizontal line is read out of the buffers, the next horizontal line is fetched from memory and loaded into the buffers. Thus, the displays are always one horizontal line behind the data retrieval from memory. This scheme allows channel data to be fetched consecutively and displayed simultaneously.
A Board Simplified Functional Description

Refer to Figure 5 on the next page for the A Board Simplified Functional Description that follows. The A Board consists of:

- Buffer and Decode Section
- Pixel Clock Generator
- Raster Read Timing Generator
- Cursor Generators
- Label Generator
- Blink Generator
- Raster Read Section
- Screen Control Section
- Prioritizer Section
- Lookup Tables Section

Buffer and Decode Section

The Buffer and Decode section links the A Board to the B Board. It buffers the 24-bit data bus and 18-bit address bus from the B Board via latches. In addition, it decodes the address bus into 24 memory mapped control signals. These signals gate memory mapped data into all blocks in Figure 5 except the TV Timing Generator.

Pixel Clock Generator

The Pixel Clock Generator generates seventeen \(24.5454514\) MHz clock signal outputs to allow short clock runs and reduce circuit loading. Most blocks of the A Board receive one or more clock signal inputs.
Figure 5. WIDE WORD A Board Functional Block Diagram
Raster Read Timing Generator

The Raster Read Timing Generator produces raster synchronization signals, blanking, gating waveforms and strobes for the workstation. It derives all timing signals from the pixel clock (24.5454514 MHz).

Cursor Generators

Two cursors are generated, one by Cursor Generator 0 and the other by Cursor Generator 1. At present, only Cursor Generator 0 is supported by software. These identical generators output a cursor bit whenever a pixel being scanned is part of a defined cursor. The cursors are moved with the PS/2's mouse. They can be one of five predefined shapes (types) with user defined heights and widths of up to 512 pixels (currently, software supports heights and widths of up to 256 pixels), or a construct of any shape that fits within a 256 x 256 pixel box. The generator's horizontal and vertical positions and type are programmed by the user via the PS/2.

The outputs of the Cursor Generators are inputs to the Lookup Tables and Prioritizer. The Lookup Tables allow masking of the cursor bits and provide cursor coloring. The Prioritizer prevents contention between the cursor bits and any other data source that may be simultaneously trying to drive the pixel currently being painted.

Label Generator

The Label Generator can provide up to 64, 16-character labels. These labels are nine scan lines high and are inserted in the last nine horizontal lines of a horizontal panel or full screen. The Label Generator contains its own 8K byte static RAM for label storage. The output of the Label Generator is a serial, single-bit data stream that is sent to the Lookup Tables section while blanking control is sent to the Prioritizer.

Characters are loaded into the Label Generator's RAM via the PS/2 and B Board. Only the last six bits of each 8-bit character are used by an output parallel-to-serial converter. The seventh bit of each character is an internal blink flag. This flag is combined with the output of the Blink Generator to blink any characters having their blink flag set. The eighth bit in each character location is unused.
Blink Generator

The Blink Generator is a 50% duty cycle square wave generator. Its frequency is user-programmable and can be set from 1/30 to 8.5 seconds per cycle. The Blink Generator output can be used with any enhancement for the Graphics Channel, Image Channel 1 or Image Channel 2. When used with the Label Generator, any or all characters in any label can be blinked. It can cause either or both cursors to change colors at the blink rate. It can also cause image and/or graphics color enhancements to change at the blink rate.

Raster Read Section

The Raster Read section sends line start addresses to the memory and reads an entire channel (up to 41 WIDE WORDs if roaming in a super frame and the zoom factor is 0). This process is repeated two more times for the remaining two channels.

To retrieve the first line of data for each of the channels in the example frame allocations described above (see page 4-2), the Raster Read section begins by sending an address of 19,200 to the memory (the starting address for image frame 2). Then, it reads the 40 WIDE WORDs and stores them in the buffer for Channel 2. Next, the Raster Read section sends an address of 00000 (the starting address of image frame 1) to the memory, reads the 40 WIDE WORDs and stores them in the buffer for Channel 1. This process is repeated once more using an address of 38,400 (the starting address for the graphics frame) for Channel 0.

Now, the next horizontal line for each channel must be retrieved. The new starting address can be computed for each channel's line by adding line length (40 in this example) to the previous start address. For Channel 2, a starting address of 19,240 is used to retrieve the next 40 WIDE WORDs. For Channel 1, a starting address of 0040 is used to retrieve its next 40 WIDE WORDs. For Channel 0, a starting address of 38,440 is used to retrieve its 40 WIDE WORDs. The Raster Read section relieves the PS/2 of the burden of supplying three new start addresses for each horizontal line by computing the new address using line length and the previous start address. Thus, the PS/2 designates a frame by a starting address and line length.
Screen Control Section

The Screen Control section controls the Dual Channel (DC) display drive. This section can configure the DC display for full screen or partition it into horizontal, vertical or quad panels. It can display a different DC input in each panel. For example, it can display Channel 0 (graphics) in the upper-left panel, Channel 1 (image 1) in the upper-right panel, Channel 2 (Image 2) in the lower-left panel, and stereo (alternating Channel 1 and Channel 2) in the lower-right panel. If all paneling is turned off, the DC display shows a full screen of a selected input channel. The Screen Control section is user programmed by commands from the PS/2 via the B Board and the Buffer and Decode section on the A Board.

The Screen Control section consists of two subsections, a panel switch section and a display control section.

Panel Switch Control Section

The panel switch control section generates horizontal and vertical switch points. During the vertical blanking period, the PS/2 loads the vertical switch point generator with the horizontal switch line value. This value is loaded into a counter which decrements at the end of each horizontal line. Upon reaching zero, the counter sets the vertical switch flag. Scan lines above the switch line form the upper horizontal panel; scan lines below the switch line form the lower horizontal panel. This flag is an input to the display control section. During the vertical blanking period, the PS/2 loads the horizontal switch point generator with the pixel switch value. At the beginning of each horizontal line, this value is loaded into a counter which decrements at the pixel clock rate. Upon reaching zero, the counter sets the horizontal switch flag. Pixels to the left of the switch point form the left vertical panel; pixels to the right of the switch point form the right vertical panel. This flag is also an input to the display control.

Display Control Section

Once partitioned by the panel switch control section, the display control section directs desired channel inputs to specific panels. Dual Channel display control is accomplished via a memory mapped 16-bit control word from the PS/2. This word is partitioned into these four sets of controls:

- display mode controls
- graphics panel masks
- image panel masks
- Window Cursor 2 control
The display mode controls describe partitioning of the Dual Channel display and are defined as follows:

- paneling off (full screen display)
- horizontal panels (display consists of top and bottom panels)
- vertical panels (display consists of left and right panels)
- quad panels (display consists of four panels: upper-left, upper-right, lower-left and lower-right)
- alternate frame stereo (full screen display: Image Channel 1 and Image Channel 2 alternate at a 60 Hz rate)
- split alternate frame (horizontal panels with alternate frame stereo in one panel and one of the three input channels in the other)
- three video channels (full screen: a third image is processed through the graphics channel and displayed on the Dual Channel)
- split three video channels (horizontal panels with a third image on one panel and graphics or Image Channel 1 or 2 on the other)

Once screen partitioning is defined, the image and graphics panel masks define which channel drives a particular panel.

Window Cursor 2, when enabled by the user, enables the Image Channel 2 input to the Dual Channel Multiplexer while scanning pixels within the Cursor 1 boundary. Thus, Window Cursor 2 is a "window" of Image Channel 2. This window, which is moved with the mouse, is useful when displaying alternate frame stereo or Dual Channels. Outside the window, the display appears as Image 1 or a combination of Image Channels 1 and 2. Inside the window, however, only Image Channel 2 is displayed. Thus, the user can observe the "Image Channel 2 only" contribution to the display.
Prioritizer

The Prioritizer section prioritizes all data inputs to all output multiplexers. Several data sources may attempt to simultaneously write to a particular pixel. For example, assume that Image Channel 1 is an image of North America and it is directed to the Dual Channel. Also assume that Channel 0 graphics is a border map of the U.S. Furthermore, Cursor 0 and the Label Generator are enabled.

There are several data conflict possibilities, e.g., image, graphics, cursor, label background and label character inputs to the Dual Channel. For any displayed pixel, you could have any combination of data sources attempting to drive the same pixel. Only one data source is allowed to write to a pixel. The Prioritizer selects the source by its priority. In decreasing priority, the data source priorities are:

- label character (highest priority)
- cursors (Cursor 0, Cursor 1 or Window Cursor 2)
- label background
- graphics
- image (lowest priority)

Lookup Tables Section

The three channel outputs of the Raster Read section are processed by the Lookup Tables section. This section forms four analog channels from the three digital channel inputs. In addition, it performs two enhancement processes. First, it enhances the channel data by supplying cursors, labels and a blink strobe. Any or all of these enhancements may be masked on or off via user controlled sets of mask gates for each channel. Second, the Lookup Tables perform an intensity-to-color lookup conversion of the input data (including cursors, labels and blink), hence its name.

Channels 0 is the graphics frame input to the Lookup Tables; Channels 1 and Channel 2 are the two image frame inputs. The four output channels are:

- Image Channel 1
- Image Channel 2
- Dual Channel
- Interlaced Dual Channel
The Lookup Tables section contains a data multiplexer and D-to-A converter for each output channel. Image Channel 1 has channels 0 and 1 as inputs. Thus, depending on what position the multiplexer is in, Image Channel 1 may write Channel 1 image data or Channel 0 graphics data to a monitor connected to Image Channel 1. Image Channel 2 can be driven by the Channel 2 image data or Channel 0 graphics data. If the optional WIDE WORD Interlace Adapter Board is installed on the A Board, Image Channel 1 and Image Channel 2 are converted to RGB interlaced format. When this board is installed, only the Dual Channel output is non-interlaced.

The Dual Channel is the normal output. It has the Graphics Channel, Image Channel 1 and Image Channel 2 as inputs. Via the PS/2's keyboard, the user can select any of these inputs or combinations of these inputs as the Dual Channel output. This output is non-interlaced and must be connected to a non-interlaced RGB monitor.

The Interlaced Dual Channel output in Figure 5 (page 4-4) is produced by passing the Dual Channel output through an interlace converter. The Interlaced Dual Channel output is usually used to drive an optional external NTSC converter. The converter's NTSC output can drive any high quality NTSC RGB monitor, recorder, etc.
A Board Detailed Functional Description

The WIDE WORD A Board Detailed Functional Description is based on Figure 6, sheets 1 and 2 on pages 4-13 and 4-14. Figure 6 is supplemented with more detailed diagrams as necessary.

The blocks in Figure 6 contain schematic sheet reference numbers that make the transition from the functional descriptions to the circuit descriptions easier. The blocks in the supplemental diagrams contain a location code that locates the IC chips that implement a specific function. The code has two numbers separated by an alpha character. The left number identifies the schematic sheet number. The alpha character and the right number are the vertical and horizontal grid coordinates, respectively. They describe the location of the chip on the sheet.

This detailed functional description describes the:

- Buffer and Decode Section
- Raster Timing Background
- Pixel Clock Generator
- Raster Read Timing Generator
- Cursor Generators
- Label Generator
- Blink Generator
- Raster Read Section
- Screen Control Section
- Prioritizer Section
- Lookup Tables Section
- Graphics Channel and Image Channels 1 and 2
- Dual Channel
- Interlaced Dual Channel
Buffer and Decode Section

Address Latch

The B Board forms 18-bit addresses and sends them to the A Board via the 50-pin JB connector. These address lines drive D-type latches that are clocked by a strobe generated on the B Board. The outputs of the latches drive the FA00-FA11 (FIFOed Address lines 00-11) bus.

Data Latch

The B Board forms a 24-bit data bus that is connected to the A Board via the 50-pin JA connector. The data bus drives transparent D-type latches that are clocked by the same strobe that clocks the Address Latch block. The output of the Data Latch drives the FD00-FD17 (FIFOed Data Bus lines 00-17) bus.

Memory Mapped Control and Strobe Delay

There are 30 registers and latches on the A Board that are memory mapped extensions of the PS/2. The FD bus presents PS/2 data (via the B Board) to each of these registers and latches at the same time. Only the register or latch whose load strobe is asserted will accept the data.

The Memory Mapped Control block decodes the upper 10 address lines of the FA address bus (FA08-FA11) into 30 address blocks. When an incoming address generates a match, that block's output load strobe is asserted, latching FD data into the memory mapped register or memory that it is connected to. The address blocks vary in size (256 words minimum) but are large enough to meet the memory mapped device's input data requirements.

The load strobes are generated after the FA address lines are stable. This is achieved by strobing the Memory Mapped Control logic gates with the input strobe from the B Board. The input strobe is delayed a few nanoseconds by the Strobe Delay block before being applied to the Memory Mapped Control block. This delay compensates for the propagation delay of the address bits as they pass through the Address Latch block.
Figure 8. A Board Detailed Functional Block Diagram (sheet 2 of 2)
Raster Timing Background

The WWW converts stored digital image and graphics data into RGB monitor outputs. To prevent display interference, all WWW evolutions involving data transfers to the A Board must be either driven by or synchronized with raster timing signals. As an example, consider the loading of an enhancement table. Even though enhancement tables are not directly displayed on the monitor, they cannot be loaded during a scan without disrupting it. Therefore, they are loaded during the vertical blanking period. At this time, the display is blanked off and nondisplay functions (such as loading of enhancement tables) can be performed without affecting the display.

Television timing and WWW timing characteristics are described below. The Raster Read Timing Generator produces all A Board timing. The Interlaced Dual Channel monitor drive output of the WWW meets all TV broadcast timing specifications. All WWW timing is directly or indirectly influenced by these specifications. Therefore, this discussion precedes the Raster Read Timing block description.

U.S. TV characteristics are the result of standards adopted by the NTSC (National Television Standards Committee). These standards are tightly adhered to by the TV broadcasting industry. A TV frame (one complete image) consists of 525 horizontal lines. Frames are generated every 1/30 second for a black and white TV and every 1/29.97 second for a color TV.

TV frames are interlaced, i.e., they consist of two fields designated odd and even. Each field has 262-1/2 horizontal lines. The even field consists of even lines only; the odd field consists of odd lines only. A field is transmitted in one-half the frame time (i.e., 1/60 second for black/white or 1/59.94 for color). The first field is written to the display, scanning every other line. Then the remaining field is written to the display, filling in between the lines of the first field. This results in an effective flicker of a 60 Hz frame rate while requiring a bandwidth of a 30 Hz frame rate.

TV horizontal and vertical sweep circuits must be synchronized to the broadcast signal. This is accomplished with horizontal and vertical synchronization signals that are transmitted as part of the TV signal. When the scan reaches the right side or bottom of the screen, the sweep circuits must return the electron beam rapidly back to the left side or top of the screen. During these return times (called flyback or retrace), the electron beam must be turned off. This is accomplished with horizontal and vertical blanking signals which shut off the beam during retrace and blank the synchronization pulse periods. The horizontal and vertical blanking periods are important in the WWW because all A Board nondisplay activity is accomplished during these times.
The vertical retrace time is approximately 21 horizontal lines per field. Thus, about 42 horizontal lines are required for each frame for the vertical retrace. This leaves 525 lines minus 42 lines for a total of 483 visible horizontal lines. The horizontal blanking period is approximately 17% of the total horizontal period.

### WWW Timing Characteristics

WWW display frames are non-interlaced. Thus, a frame and a field are the same thing. To prevent flicker, the frame rate is doubled from 30 Hz for interlaced TV frames to 60 Hz for the non-interlaced WWW. This requires doubling of the horizontal scan rate. Instead of 15,734 horizontal lines/second \((29.97 \text{ frames/second} \times 525 \text{ lines/frame} = 15,734)\), a WWW generates 31,468 horizontal lines/second. Thus, to maintain the same horizontal pixel resolution, data must be written twice as fast for a WWW as it is for interlaced TV. Vertical and horizontal blanking ratios are maintained at 42 horizontal lines and 17% of each horizontal line, respectively.

### Timing Comparison

WWWs produce an interlaced color monitor drive from the Dual Channel non-interlaced drive signal. Comparing the two sets of timing characteristics in Table 3 below will suggest a simple approach for converting the Dual Channel drive to the interlaced format.

<table>
<thead>
<tr>
<th>Fields/Frame</th>
<th>H.Lines/Field</th>
<th>H.Scan Rate</th>
<th>V.Scan Time</th>
<th>H.Blank</th>
<th>V.Sweep Blank</th>
</tr>
</thead>
<tbody>
<tr>
<td>TV 2</td>
<td>262.5/Field</td>
<td>63.55μs</td>
<td>59.94Hz</td>
<td>17%</td>
<td>21/Field, 42/Fr.</td>
</tr>
<tr>
<td>WWW 1</td>
<td>525/Frame</td>
<td>31.78μs</td>
<td>59.94Hz</td>
<td>17%</td>
<td>42/Frame</td>
</tr>
</tbody>
</table>

**Table 3. Timing Comparisons**

By buffering every other horizontal line of the WWW data and writing that data at one-half the WWW horizontal rate, one TV field (262.5 even or odd lines) is generated during a WWW frame. If this process is repeated during the next WWW frame, the other TV field is generated, completing the TV frame. The only remaining modifications are the generation of composite horizontal and vertical sync and blanking. Separate horizontal and vertical sync and blanking signals are generated for the Interlaced Dual Channel output.
Pixel Clock Generator

The Pixel Clock Generator provides the time base for the workstation. All timing originates directly or indirectly from this generator. It produces seventeen 24.5454514 MHz outputs to drive the large number of A AND B board components requiring a clocking input. This generator consists of a Clock Oscillator which generates the 24.5454514 MHz signal, a Buffer to minimize oscillator loading, and Drivers to increase the fan out. The outputs are labelled PXLCK-A through PXLCK-Q. Note in Figure 7 that PXLCK-O drives the Raster Read Timing Generator. Throughout the remainder of the functional descriptions, all clock outputs are referred to as "pixel clock."

Raster Read Timing Generator

Refer to Figure 7 on the next page and Sheet 1 of Figure 6. Each signal from the Raster Read Timing block is described briefly below.

Odd/Even Line

The Odd/Even Line signal changes state with the beginning of each non-interlaced horizontal line. It is used by the interlace logic to gate every other horizontal line into the Interlace FIFO (buffer). Thus, two 525-line non-interlaced frames are required to generate one interlaced frame (two interlaced fields of 262-1/2 lines each).

Line Gate

The Line Gate is asserted during the visible pixel time for each horizontal line. The time begins with pixel 128 and ends with pixel 767. This signal is used by the Pixel Selector blocks (one for each channel) and the Vertical Panel Switch Generator.

Composite Blanking

Composite Blanking is a composite of horizontal and vertical blanking. This signal blanks non-interlaced monitors during the horizontal and vertical retrace times. These signals are generated in the same manner as the Composite Sync signal. However, their durations are slightly longer. Horizontal blanking leaves about 647 visible pixels when a line is defined as 780 pixels (horizontal blanking is approximately 17% of the horizontal cycle). A field typically consists of about 483 horizontal lines (vertical blanking is approximately 42 horizontal lines in duration). In the WWW, horizontal and vertical blanking is increased slightly to limit the display frame size to 640 pixels by 480 lines.
Figure 7. Raster Read Timing Generator
Composite Sync

Composite Sync consists of horizontal and vertical sync signals. These signals are required by the RGB monitors connected to the non-interlaced output channels (Image Channel 1, Image Channel 2 and the Dual Channel). Composite Sync is produced by combining vertical and horizontal sync pulses. The horizontal sync component's logic is driven by the parallel outputs of a counter driven by pixel clock that counts to 779 and resets. Thus, a horizontal scan period is defined as 780 pixel clock periods. The logic combines various count combinations to generate the horizontal sync pulses. The horizontal sync pulse actually begins before the end of the current scan to allow time for the monitor's sweep circuits to respond.

The vertical component of the Composite Sync is a series of pulses called a serrated sync pulse. This signal is enabled only during horizontal lines 6-11. During this time, six vertical sync pulses (equals one serrated vertical sync pulse) are generated by counting a specific number of pixel clock pulses during each horizontal line time. The serrations provide the monitor with horizontal sync information during the vertical sync period.

Interlaced Sync and Blanking

The Dual Channel's output signal is available at the rear of the WWW in either a non-interlaced or interlaced format. The interlaced signal is generated by buffering lines of non-interlaced signals and outputting this data at the interlaced rate. In addition to the image data, composite interlaced sync and blanking signals are required. These signals cannot be derived by processing the non-interlaced Composite Sync and Blanking signals in the same manner that the interlaced image data is derived.

The Interlaced Composite Sync and Blanking signals are generated directly by the Raster Read Timing section. These signals are required by the Interlaced Dual Channel DAC. In addition, the Interlaced Dual Channel Sync is an output to the workstation's rear panel. It is required by the interlace monitor or encoder (see sheet 2 of Figure 6).

If the optional WIDE WORD Interlace Adapter Board has been plugged onto the A Board, interlaced sync and blanking signals are routed to the Interlaced Image Channel 1 and Image Channel 2 DACs located on the daughter board. Installation of the daughter board also automatically disconnects the non-interlaced Channel 1 and Channel 2 Sync Drivers (see sheet 2 of Figure 6) from their output BNC connectors. These connectors are now driven by the Channel 1 and Channel 2 Sync Drivers located on the daughter board. Thus, interlaced sync is available at the Interlaced Dual Channel, Image Channel 1 and Image Channel 2 BNC output connectors.
A Board access time is variable and may end as late as 20.5 usec into the horizontal cycle time. Read/Write Enable (labeled R/W ENABLE in Figure 7) multiplexes A and B read/write access to the WIDE WORD memory. When it is low, the A Board has access to the memory; when it is high, the B Board can access the memory. Read/Write Enable goes low at the beginning ofRaster Read Start. It goes high after the A Board read cycles finish and remains high until a few microseconds after the start of the next horizontal line. This ensures that any Dataram access cycle initiated by the B Board before the end of the current horizontal line completes.

External Refresh

The dynamic RAMs in the Dataram WIDE WORD memory must be refreshed periodically. The Dataram memory can be configured for internal or external refresh control. External refresh control is used to eliminate interference caused by refreshing the memory asynchronously. In the WWW application, all refreshing is performed during the horizontal blanking periods. External Refresh enables the Dataram's internal refresh generator only during pixels 20-59 of each horizontal line. This allows three refresh cycles at the beginning of each 31.77 usec horizontal line.

Raster Read Start

Shortly after the end of the External Refresh gate, the Raster Read Start pulse is generated. This pulse, lasting one pixel clock period, initiates the Sequential Read cycles for retrieving the next horizontal line's data. The data for the current line was retrieved during the previous horizontal line and stored in temporary buffers.

The Raster Read process consists of three Sequential Read cycles, one for each channel. Raster Read Start initiates the first cycle. The end of the first cycle initiates the second cycle; the end of the second cycle initiates the third. Each cycle retrieves up to 41 WIDE WORDs. Each cycle has a 480 nsec Sync phase, followed by a variable length read cycle and ending with a 480 nsec Ending Sequence. The variable read cycle equals 120 nsec per WIDE WORD. Thus, if all three channels retrieve 41 WIDE WORDs each (worst case), the Raster Read process requires about 17.28 usec. Including the refresh time, the Raster Read process ends at about 20.5 usec after the start of the horizontal line (31.77 usec in duration).
Frame Interrupt
Frame Interrupt (labeled FRAME INT in Figure 7) is produced by dividing the vertical frame rate (1/59.94 seconds/frame) by two (1/29.97 seconds/frame). This signal serves as a PS/2 interrupt. It tells the PS/2 that a frame has ended and a vertical retrace is in progress. During this time, such parameters as cursor size and position, lookup table reloading, frame starting addresses, display modes and Label Generator programming are accomplished. These parameters are loaded into B Board to A Board Data FIFOs during picture display time and are transferred (read from the FIFOs) during the vertical blanking period. Thus, they do not affect the display.

Label Start Line
The Label Start Line marks the beginning of the bottom label field. This signal goes true for the ninth horizontal line before the bottom line of the frame. It marks the beginning of the full screen and bottom panel split screen label fields. Since the top panel is variable in height, this circuit cannot generate the start of the upper panel's label field.

Vertical Gate
The Vertical Gate is asserted from horizontal lines 0 through 42. Due to the vertical blanking portion of Composite Blanking, horizontal line 44 is the first visible horizontal line. During the Vertical Gate period, color enhancement tables, cursor parameters, the frame and/or panel start address, blink parameters, zoom factors, and display modes are reloaded. Because of the quantity of data required to update the Dual Channel Palette RAM, it is reloaded over several Vertical Gate periods.

Vertical Drive
The Vertical Drive is asserted from horizontal lines 6-11. This signal is a component of the Composite Sync signal used by the channel D to A converters. Vertical Drive is required by some monitors (e.g., Zenith model 1432) for proper lock. The Vertical Drive is buffered and output to a BNC connector on the rear panel of the WIDE WORD Chassis. This signal is useful as an oscilloscope sweep trigger during troubleshooting.
Cursor Generators

The A Board contains two Cursor Generators labeled Cursor 0 and Cursor 1. Since these generators are identical, only Cursor 0 is described here.

Cursor 0 has a serial output (CUR0) that is asserted whenever a Cursor 0 pixel is painted. The output is applied to the Prioritizer and Lookup Tables. When CUR0 is asserted, the Prioritizer determines if CUR0 is the highest priority data competing for the pixel (only the Label character is higher). If CUR0 is the highest priority data and it is masked on, it is gated through a specified channel multiplexer and paints the current pixel.

Cursor 0 receives horizontal and vertical position data, and cursor size and type information from the PS/2 via the B Board. This data is transmitted to Cursor 0 during each vertical blanking period. Cursor 0 generates the cursor in the same location for every frame until the PS/2 changes one or more parameters, e.g., position, size or type.

The Cursor Generator is actually two state machines. One controls vertical position and size; the other controls horizontal position and size. Vertical and horizontal positioning via the PS/2's mouse can place the cursor anywhere on the screen. However, once the cursor's center pixel reaches the edge of the screen, the mouse is not allowed to move the cursor further off screen. Internally, the state machines define a rectangular box having a maximum horizontal or vertical size of 512 pixels. Cursor logic identifies the following attributes of this box:

- upper-left pixel
- top line
- top line - center pixel
- left side
- vertical center line
- right side
- left side - center pixel
- horizontal center line
- center pixel
- bottom line
- solid box (excludes perimeter pixels)
- top center line (from top of box to top of screen)
bottom center line (from bottom of box to bottom of screen)
left center line (from left edge of box to left edge of screen)
right center line (from right edge of box to right edge of screen)

One or more of these attributes may be selected to define the displayed cursor. For example, selecting the horizontal and vertical center lines to define the displayed cursor specifies a cross hair. The height and width of this cross hair are determined by the rectangular box size. Internal logic provides these five standard cursors:

- box (all perimeter lines)
- cross hair (vertical and horizontal center lines)
- box and cross hair
- solid box
- Star Wars gun sight (all perimeter lines plus the center pixel plus the top, bottom, left and right center lines)

Figure 8 on the next page shows these cursors. Cursors are selected with commands from the PS/2. In the event that no standard cursor meets a user's needs, a cursor of any shape can be generated by programming a cursor Construct RAM in the Cursor Generator (maximum size is 256 by 256 pixels). This RAM must be reloaded if the cursor height or width is changed. The constructed cursor along with its complement are available for selection. When the constructed cursor's complement is selected, CUR0 is asserted for all areas outside the defined cursor as well as those unprogrammed areas inside the cursor perimeter. In effect, this generates a display window.

Note, as of this revision date, mainframe and PS/2 software do not support the constructed cursor programming. Thus, the constructed cursor and its complement are not currently useable.
Figure 8. Cursor Types
Horizontal and Vertical State Machines

Refer to Figure 9, on the next page. Since the horizontal and vertical state machines are similar in operation, only the Horizontal State Machine is described in detail here. If you replace the words "left" with "top," "right" with "bottom," "horizontal" with "vertical," and "width" with "height," the Horizontal State Machine description is completely valid for the Vertical State Machine. The Horizontal State Machine consists of:

- Start Latch (located at 4D7)
- Width Latch
- Horizontal Counter
- Horizontal State Counter
- part of the State Decode PALs* block

Start Latch

The Start Latch is a memory mapped extension of the PS/2. It is loaded with the cursor's left-most display pixel address during the vertical blanking period. Its contents are enabled onto the Horizontal Counter preload bus prior to the beginning of every horizontal line by an enable output from the Raster Read Timing Generator block.

The cursor can be moved off-screen to the point that the cursor's center pixel is coincident with an edge of the display. If the cursor is moved partially off the left edge of the screen, the Start Latch function may not be needed. This happens when the portion of the cursor that is off-screen is equal to or greater than the horizontal blanking period (128 pixels). Under this condition, the Start Latch is used to store the cursor's first half-width and the Width Latch stores the cursor's last half-width. Refer to the Width Latch description below for more information.

Width Latch

The Width Latch is a memory mapped extension of the PS/2. It is loaded with a value equal to the cursor's width divided by two. The output of this latch is enabled onto the Horizontal Counter preload bus when the left edge of the cursor is reached, and again when the vertical center line is reached.

If the cursor's offset reduces to zero while moving the cursor off the left edge of the display as described above, the contents of the Start Latch are loaded into the Horizontal Counter in lieu of the Width Latch contents. Under this condition, the latch's contents are loaded into the Horizontal Counter only when the vertical center line is reached.

*PAL is a registered trademark of Monolithic Memories, Inc.
Figure 9. WIDE WORD A Board Cursor Generators
The Horizontal Counter locates the left edge of the cursor and determines the cursor's half-width by counting pixels. Since the left edge of a cursor can occur at pixel counts greater than 512 (measured from HCR), a 10-bit binary counter is required. For location of the left edge only, the 8-bit binary Horizontal Counter is cascaded with the Horizontal State Counter to form a 10-bit counter. Once the left edge is located, the two counters are disconnected from each other. Operating in its 8-bit mode, the counter can count a half-width of 256 pixels (cursor width of 512 pixels).

Prior to the start of each horizontal line, the contents of the Start Latch are loaded into the Horizontal Counter. It operates in the decrement mode and is clocked by pixel clock. When it reaches zero, the left edge pixel column has been reached. The contents of the Width Latch are loaded into the counter. The counter decrements and upon reaching zero indicates the vertical center line pixel has been reached. The counter is preloaded with width data once more and allowed to decrement to zero. This time, the right edge pixel column has been reached. This process is repeated for each of the 480 visible horizontal lines.

The Horizontal State Counter is a 4-bit binary counter (only the 3 LSBs are used) that is loaded at the start of each horizontal line. It provides cursor location information to the State Decode PALs block. The third LSB of this binary down counter is loaded with the Edge Flag; its two LSBs are preset with the 2 MSBs of the Start Latch (left edge pixel count). The State Decode PAL interprets the 2 LSBs of counts 6 - 4 as the 2 MSBs of the Horizontal Counter. It interprets counts 3 - 0 as the horizontal state count. The output of this counter is used with the Horizontal Counter's underflow signal which is asserted each time the Horizontal Counter reaches zero. Table 4 below defines all possible state and underflow combinations.

<table>
<thead>
<tr>
<th>Horizontal State</th>
<th>Underflow</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>1</td>
<td>left of cursor's left edge</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>at left edge</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>between left edge and center line</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>at center line</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>between center line and right edge</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>at right edge</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>right of cursor's right edge</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>invalid combination</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>prohibited state</td>
</tr>
</tbody>
</table>

* 0 = asserted, 1 = not asserted, X = don't care

Table 4. Cursor Horizontal State Code Definitions
**Edge Flag Latch**

The Edge Flag Latch defines the function of the two LSB outputs of the Horizontal State Counter. If the flag is low, the two LSBs represent the horizontal state (binary counts 0011, 0010, 0001 or 0000); if the flag is high, the two LSBs represent the two MSBs of the horizontal offset position (binary counts 0110, 0101 or 0100). It's possible to use the Horizontal State Counter for both functions because state codes greater than 4 (0100 binary) are undefined and a state code of 4 indicates "left of cursor's left edge" (see Table 4).

If the cursor's width is greater than 256 pixels (half-width is greater than 128 pixels), it is possible for the horizontal offset to reach zero before the cursor's center pixel reaches the left edge of the display (end of travel in the left direction). If this happens, the state code must be preset to a value less than 4 to indicate that the start of the horizontal line is within the cursor field. Thus, the state code must be programmable.

The Edge Flag Latch latches the 0A bit on the Data Bus at the time the horizontal offset is latched into the Horizontal Start Latch. The Edge Flag output is the MSB preset input to the Horizontal State Counter. The Horizontal State Counter passes this bit to the State Decode PALs (MSB) which use it to interpret the two LSB inputs from the Horizontal State Counter.

**State Decode PALs**

The State Decode PALs (Programmable Array Logic) block is common to both state machines.

This programmable device assembles cursor horizontal and vertical attributes and state machine states to form the five standard cursors shown in Figure 8. It also forms the constructed cursor and its complement. Thus, there are seven possible cursors for users to select.

Cursor selection decoding is the final function of the State Decode PALs block. Cursor selection by the user results in a PS/2-generated Cursor Type control word. The PS/2 writes the Cursor Type to a 3-bit memory mapped register in the State Decode PALs block. This data is carried on the FD00-FD02 data bus lines. The State Decode PALs decode the 3-bit word to enable one of the cursors onto the Cursor Bit output line. Table 5 on the adjacent page describes the decode function.
The horizontal and vertical cursor attributes available to the State Decode PALs limit cursor forms to combinations of horizontal and vertical lines. When more complicated forms, such as those having curves, circles and diagonal lines, etc., are required, a cursor of any shape that will fit inside a 256 x 256 pixel box may be constructed.

The constructed cursor is stored in the Construct RAM, a 64K by 1-bit static RAM. RAM addressing is multiplexed. During programming by the PS/2 user, the RAM is a memory mapped extension of the PS/2. Since only the LSB of the FD bus supplies data to the RAM, 64K of addressing space is required to program the 64K bits of the RAM. During cursor display, the Construct RAM is addressed by the Vertical and Horizontal Counters. The RAM is programmed as four quadrants of 128 rows of 128 pixels because the counters function as down counters that define half width and half height. During display, these counters are each loaded twice as is done when displaying one of the standard forms.

During display of the constructed cursor, the Horizontal and Vertical Counters drive the RAM’s address lines. The Horizontal Counter drives the eight LSBs; the Vertical Counter drives the eight MSBs. This partitions the RAM into four quadrants; see page 5-24 for more information. When the constructed cursor is selected (cursor type 6), the output of the Construct RAM is enabled whenever the scan is inside the cursor rectangle defined by the Horizontal Start and Width Latches and the Vertical Start and Height Latches.
Figure 10. Label Generator Functional Block Diagram
Label Generator

The Label Generator can write up to two 106-character labels per displayed frame. It has internal label storage (static RAM) for up to 32 display frames. Thus, it can store up to 64, 106-character labels. During storage, the RAM is a memory mapped extension of the PS/2.

In the split screen mode (containing an upper and lower panel), two label fields are generated. The label field consists of the last nine horizontal lines of a panel or screen. Each field is divided into blocks six pixels wide. This results in a label field with 106 character fields, each six pixels wide by nine rows high. The upper and lower label field lines are reserved for background, resulting in seven lines for character use. The sixth pixel in each character field is reserved for background. The result is an active character field of 5x7 pixels.

Refer to Figure 10 on the adjacent page. The Label Generator consists of:

- Character RAM
- Character and Pixel Counters
- Character PROM
- Line Counter
- Output Shift Register
- Blink Control

Character RAM

The Character RAM is an 8K byte static RAM partitioned as 64, 128-byte memory blocks. Each block stores one 106-character label. Thus, there are 22 unused bytes in each block. The RAM's address lines are driven by a multiplexer. During label storage, the multiplexer allows the PS/2 to address the RAM. At this time, PS/2 data (via the B Board) passes through the Data Buffer to the RAM's I/O data bus and into the RAM.
The output of the Address Multiplexer addresses the Character RAM. Its two sets of inputs are the FA (FIFOed Address) bus and the FD (FIFOed Data) bus. During character storage, the lower 13 bits of the FA bus are gated through the multiplexer.

Prior to the start of a frame, the Latch block is loaded with the label number. This block is a memory mapped register. Its 5-bit output drives bits 8-12, respectively, of the Character RAM during label readout. Since bits 1-7 function as a character address (0-127 range), the Latch's output functions as a 1 of 32 label addresser.

The Character RAM's Bit 13 drives the Top/Bottom Gate (TBG) signal during character readout and functions as a bank select. When TBG is low, the lower bank of 32 labels is available; when TBG is high, the upper bank of 32 labels is available. The lower bank stores labels for full screen displays and the upper panel in the split panel mode. The upper bank stores labels for the lower panel in the split screen mode.

The Character Counter and Divide-by-Six Pixel Counter provide an address to the Address Multiplexer during label readout. In addition, the Pixel Counter provides a load pulse for the Output Shift Register.

The Divide-by-Six Pixel Counter is a binary down counter that is preset to five and clocked by pixel clock. It underflows on every sixth clock pulse, reloading itself and clocking the load pin on the Output Shift Register. One of the counter's Q outputs drives the clock input of the Character Counter. This Q output functions as a character clock since six pixels make up the width of each character field.

The Character Counter is a 7-bit, binary up-counter. Its seven output lines drive the seven LSBs of the Character RAM via the Address Multiplexer during label readout.
The Character PROM presents a bit pattern code to the Output Shift Register for each line of each displayed character in the label. The first label line is a background line. It is blanked by the Prioritizer and not processed by the Label Generator. The remaining eight lines, including the last background line, are driven by the character PROM.

Each character's code is presented to the Character PROM eight times, once during each line. Thus, there are 848 (106 characters x 8 lines/characters = 848) Character PROM lookups during the display of each label. The Character PROM uses the character code to address an 8-byte character lookup table. The output of the Divide-by-Eight Line Counter points to the specific byte in the character's lookup table to be sent to the Output Shift Register. The 6-bit output of the Character PROM represents the six horizontal pixels of the next character to be displayed. This code is latched into the shift register and serially shifted out at the pixel clock rate.

The Divide-by-Eight Line Counter generates a 3-bit line count that is used by the Character PROM as a character lookup table pointer. This block is enabled only during the label field by the Label Display Start input. Once enabled, the counter increments on the rising edge of the Horizontal Line Gate, an output of the Raster Read Timing block.

The Output Shift Register converts the parallel bit pattern inputs to a serial data stream. The serial output is clocked (shifted out) at the pixel clock rate. At all times, the Output Shift Register is either in the shift right mode or the load mode. The mode is determined by the status of the Load input. When Load is low, the shift register is loaded with the next bit pattern code on the next rising edge of pixel clock; when Load is high, the bit pattern is shifted one bit toward the LABEL CHAR output on each rising edge of pixel clock. As each bit is shifted out, a low is shifted in. This feature is used with the Blink Control.
Blink Control

The Blink CTL (Control) block, when enabled, causes the Output Shift Register not to be reloaded with a new bit pattern code at the end of the current character. This causes the lows that were shifted into the Output Shift Register, as the current character was shifted out, to be shifted into the output. Thus, when Blink is active, the Output Shift Register continuously outputs background (low output). This replaces the character with background. Blink is active when the Blink Strobe and the character's bit seven output are simultaneously high. Since the Blink Strobe toggles at a programmable rate (see the Blink Generator description below), the character flashes (blinks) if its bit seven is high.

Blink CTL is driven by the programmable Blink Generator and bit seven of the character code. The Character PROM requires a 6-bit character code for character identification. It uses Character RAM bits 0-5 for this purpose. Character RAM bit six is unused and bit seven functions as a blink flag. If the user wants a character to flash, that character is sent to the Character RAM with bit seven set high. This bit acts as a Blink enable when the character is read from the Character RAM.
Blink Generator

The Blink Generator provides a 50% duty cycle square wave to the Character Generator and the Cursor/Blink/Character Latch (see Sheet 2 of Figure 6 on page 4-14). It has a memory mapped rate range of 1/30 to 8.5 seconds per cycle.

The Blink Generator's output (BINK) is used by the Label Generator to flash tagged label characters. It also drives the Cursor/Blink/Character Latch which in turn drives the Graphics, Image Channel 1 and Image Channel 2 with CUR0, CUR1, CHGN and BINK. These signals, via the respective channel mask gates and latches, drive addressing inputs of the Graphics, Image Channel 1 and Image Channel 2 enhancement tables. For each channel, two full sets of enhancement table areas exist, one with BINK off and one with BINK on. Thus, a different set of image and graphics enhancements may be programmed for use with the Blink Generator. Some of the possibilities are:

- changing graphics colors at the blink rate
- changing color enhancements of images at the blink rate
- changing cursor colors at the blink rate
Figure 11. Typical Standard TV Frame to Dataram Memory Map
Raster Read Section

To help you better understand the Raster Read section, these features unique to the WWW are described below:

- line length
- zoom factors
- roaming

A standard TV frame consists of 480 lines of 640 pixels each. Since each WIDE WORD consists of 16 pixels, a standard TV frame consists of 480 lines of 40 WIDE WORDs each.

Line length is the number of WIDE WORDs required to store each frame line. For a standard TV frame, this number is 40. Line length is a frame parameter. If you are zoomed in, each line uses less than 40 WIDE WORDs, but the line length is still 40 for a standard TV frame.

The Raster Read line start addresses are computed for each channel by adding line length to each channel’s previous line start address. Figure 11 on the adjacent page shows how a standard TV image frame is stored in memory. The frame begins at address 00000 in memory and ends at 19,199 (480 lines of 40 words each). Addresses shown in Figure 11 are in decimal for simplification.

As an example of the use of line length (40 words in Figure 11), assume you have just completed scan line 1. Thus, you have displayed WIDE WORDs 0-39. The pixel to be displayed directly below pixel 0 of scan line 1 resides in the first byte of WIDE WORD 40. The starting address for the line you just completed (scan line 1) is 0. If you add the line length to the previous start address, you get 40. This address is sent to the Dataram memory as the new start address. The first byte of the first word in scan line 2 (first byte in word 40) contains the pixel to display directly under pixel 0 of scan line 1.

Zoom factors are entered by the user into the PS/2. From the PS/2, the zoom factor is sent to the A Board’s Raster Read Line Length and Zoom Factor Files block (see Figure 6).
The zoom factor is an integer from 0 to 15. The zoom factor magnifies a portion of the frame. Zoom is accomplished by duplicating pixels (resulting in horizontal magnification) and lines (resulting in vertical magnification) an integer number of times. The magnification factor is applied equally to the horizontal and vertical dimensions of the frame. The magnification factor for each dimension is the zoom factor plus one, giving a horizontal and vertical range of 1-16. The true magnification factor is a product of the horizontal and vertical magnification factors. Table 6 below shows the resulting magnification factors.

<table>
<thead>
<tr>
<th>Zoom Factor</th>
<th>Magnification</th>
<th>Zoom Factor</th>
<th>Magnification</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>8</td>
<td>81</td>
</tr>
<tr>
<td>1</td>
<td>4</td>
<td>9</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>9</td>
<td>10</td>
<td>121</td>
</tr>
<tr>
<td>3</td>
<td>16</td>
<td>11</td>
<td>144</td>
</tr>
<tr>
<td>4</td>
<td>25</td>
<td>12</td>
<td>169</td>
</tr>
<tr>
<td>5</td>
<td>36</td>
<td>13</td>
<td>196</td>
</tr>
<tr>
<td>6</td>
<td>49</td>
<td>14</td>
<td>225</td>
</tr>
<tr>
<td>7</td>
<td>64</td>
<td>15</td>
<td>256</td>
</tr>
</tbody>
</table>

Table 6. Zoom and Magnification Factors

If you display the standard TV frame shown in Figure 11 at a zoom factor of 0 (times one magnification), you can display the entire frame (640 pixels x 480 lines = 307,200 pixels or 19,200 WIDE WORDs). If you switch to a zoom factor of 15, only a small window of the standard TV frame can be displayed. Within this window, each pixel and line is repeated 16 times. Thus, only 40 pixels of 30 lines (1200 pixels total) can be displayed. Assuming a start location of zero, this zoom factor (15) replicates the first 40 pixels of the first 30 lines to fill the entire display. Figure 12 on the adjacent page shows the zoom effect.

Zooming is not very useful without some method of controlling which portion of the stored frame to magnify. The roam feature allows the user to move the magnification window to any part of the stored frame using the PS/2's mouse. If the zoom factor is zero and the stored frame is a standard TV frame, roaming is not allowed because the perimeter of the magnification window is coincident with the perimeter of the TV frame on all four sides. However, roaming can be used with a zoom factor of zero in super frames. Roaming can also be performed at zoom factors greater than zero for all frames.
Horizontal roaming is accomplished by changing the pixel starting address; vertical roaming is accomplished by changing the start line. If the pixel starting address change is not modulo 16 (e.g., 1-15, 17-31, 33-47, etc.), one extra word must be read from memory for each line.

To demonstrate, assume that you are working in a super frame with a line length of 80 words and 960 lines (four times as large as a standard TV frame). Also assume that the zoom factor is zero. Now, via the mouse, you move (roam) the display one pixel to the right in the super frame. When you retrieve the first word of a line, you must point at the second byte (instead of the first) to represent the first displayed pixel. Thus, you use only 15 bytes from the first WIDE WORD and paint the first 15 pixels. You use all 16 bytes of the next 39 WIDE WORDS. You must read one more WIDE WORD (41st word of this line) and use only the first byte to finish the line for a total of 640 pixels. The remaining 15 bytes are flushed.
The Raster Read section introduced in Figure 5 and described in the WIDE WORD A Board Simplified Description section consists of the following blocks in Figure 6:

- Raster Read Start Address File
- Raster Read Line Length and Zoom Factor Files
- File Address Multiplexer
- Raster Read Address Generator
- WIDE WORD Address Bus Drivers
- Raster Read Sequence Control
- WIDE WORD Data Latches
- Channel A, B and C FIFOs
- Channel A, B and C Pixel Selectors

These blocks are described below.

Raster Read Start Address File

The Raster Read Start Address File stores the starting address of each channel. There are three channels, each of which may contain two starting addresses. The dual start address capability allows each channel to display a different frame in the upper and lower panel. Thus, six starting addresses can be loaded into the file.

Because of the large Dataram memory storage capability, 32 output address lines are required. Since the FD bus is only 24 bits wide, two FD bus words and two latch strobes are required to store each start address. The start addresses are carried on the FD bus and loaded into the file (the files are RAM locations) by either the Upper Start Address (USA) or Lower Start Address (LSA) strobe. Effectively, the Raster Read Address File functions as a 6-word by 32-bit RAM.

The Load Address bus (LA0-LA2) addresses one of the six file locations during address loading and retrieval. Additional Raster Read Start Address File addressing information is provided in the File Address Multiplexer description below.
The Raster Read Line Length and Zoom Factor Files block stores a frame line length and zoom factor for each Raster Read Start Address File location. Since both blocks are addressed by the same LA bus, they present their outputs to the Raster Read Address Generator in synchronism. Thus, each raster read start address has an associated line length and zoom factor.

The Raster Read Line Length and Zoom Factor Files block is loaded with 16-bit line lengths from the FD bus on the rising edge of the Line Length Load (LLL) strobe. The zoom factors are loaded from the FD bus on the rising edge of the Zoom Factor Load (ZFL) strobe. A raster read start address, line length, and zoom factor are used by the Raster Read Address Generator to generate the starting address for each horizontal line of each channel.

The Raster Read Start Address File and the Raster Read Line Length and Zoom Factor Files blocks require file addressing from two sources. They are addressed by the PS/2 (via the FA bus) during file loading; they are addressed by the Raster Read Sequence Control block during unloading. Address source switching is performed by the File Address Multiplexer. Since all PS/2 to A Board data transfers occur during the vertical blanking period, Vertical Gate (see page 4-21) is used for multiplexer switching. Thus, the PS/2 drives the LA bus during vertical blanking and the Raster Read Sequence Control block and Top/Bottom Gate (TBG) drive the LA bus during visible line scanning.

The Line Start (LS0-LS1) bus output of the Raster Read Sequence control block functions as a channel selector (Channels 0-2); TBG functions as a low/high start address selector (TBG is low or high, respectively) for the selected channel. Together, these two address sources provide a 0-5 addressing range. Table 7 below summarizes the multiplexer’s output during visible line scanning.

<table>
<thead>
<tr>
<th>LS1</th>
<th>LS0</th>
<th>TBG</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Channel 0 lower start select</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Channel 0 upper start select</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Channel 1 lower start select</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Channel 1 upper start select</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Channel 2 lower start select</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Channel 2 upper start select</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>not used</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>not used</td>
</tr>
</tbody>
</table>

Table 7. Start Address File Addressing
Figure 13. Raster Read Address Generator
Figure 13 on the adjacent page is the Raster Read Address Generator functional block diagram. This block computes the line start address for each channel from the following parameters:

- full screen or panel start address (Raster Read Start Address File output)
- line length
- zoom factor

The Raster Read Address Generator computes the next start address for a channel by adding that channel's line length to its previous start address. This process is performed three times during each horizontal scan, once for each channel. It is effected by the zoom factor since zoom factors greater than zero involve line replication, i.e., a zoom factor of three results in each line being written four times.

Here is an example of how it works. Refer to Figure 13 while reading this example. During the last blanked vertical line, Channel C's Raster Read Start Address (full screen or upper horizontal panel), line length and zoom factor (Image 2) are presented to the Raster Read Address Generator. The output of the Line Length Multiplexer (MUX) is zero and the Previous Address FIFO's output is tri-stated. Thus, the output of the Adder is equal to the Raster Read Start Address input. This output is sent to the Dataram memory. It is also loaded into the Previous Address FIFO. The Channel C data is retrieved.

During the Sequential Halt cycle that follows the Sequential Read cycle, Channel B's Raster Read Start Address, its line length and zoom factor are presented to the Raster Read Address Generator in the same manner as for Channel C. Thus, at this time, the Previous Address FIFO has two entries. Channel B's data is now retrieved. During Channel B's Sequential Halt cycle, Channel A's (Graphics) start address is stored as described above for Channels C and B. The Previous Address FIFO now has three entries, and three lines of data have been retrieved and stored in the Channel C, B and A FIFOs.

The Raster Read Start File output is now tri-stated and the Previous Address FIFO is enabled. Thus, the A input of the Adder is multiplexed. It is driven by the Raster Read Start Address File during the initial load for the full screen and/or panels. At all other times, it is driven by the output of the Previous Address FIFO. The current output of the Previous Address FIFO is the address stored for Channel C (the first address stored during the previous line). The B input of the Adder is driven by the Line Length Multiplexer (MUX). The function of the Line Length MUX is effected by the zoom factor which is either zero or nonzero.
When the zoom factor is zero, the Line Length MUX passes the line length input to the B input of the Adder. Since the A input is currently driven by the initial Channel C start address, the Adder's output is Channel C's Start Address plus its line length. This new address is stored in the Previous Address FIFO for use during the next line. It is also sent to the Dataram memory as described above. Next, the Previous Address FIFO is read, enabling the next channel's previous address (Channel B's start address) to the Adder's A input. Channel B's Line Length File is enabled via the Zero Line Gate (ZLG). Thus, at this time, the Adder's output equals Channel B's Start Address plus its line length. This address is stored in the Previous Address FIFO and sent to the Dataram as described above. This address generation process is repeated for Channel A. Upon completion of the Channel A address generation, the Previous Address FIFO again has three entries, but these entries represent the previous start address plus the respective line length. This entire process repeats until a new Raster Read Start Address is received or the frame ends.

What actually occurred in this example was that each line of each channel was retrieved zoom factor plus one times. Since the zoom factor was zero, each line was retrieved once. For nonzero zoom factors, each line of each channel must still be retrieved zoom factor plus one times. For example, if a channel's zoom factor is three, the same line is retrieved four times. The same line is retrieved by adding zero instead of the line length to the previous start address. The start address doesn't change and the same line is retrieved again.

The Zoom Factor State Machine controls the number of line repetitions for all three channels. It functions as three independent, presettable, self-loading down counters. These counters are initially preset with the zoom factor at the beginning of each frame or panel. The counters decrement at the horizontal line rate and are preset to the zoom factor each time they decrement to zero. Each time a counter is preset, the state machine's output selects the line length input to the Line Length MUX as the Adder's B input. At all other times, zero is selected.

**WIDE WORD Address Bus Drivers**

The 32-bit addresses generated by the Raster Read Address Generator are composed of a byte pointer (least significant 4 bits) and a 28-bit WIDE WORD address (upper 28 bits). The WIDE WORD Address Bus Drivers block uses the 28-bit WIDE WORD addressing component to drive inverting amplifiers that address the 28 least significant address lines of the Dataram memory. The WIDE WORD Address Bus Drivers drive a total of 32 bits. The four MSBs are not used in the workstation application of the WIDE WORD memory. These bits normally daisy chain multiple WIDE WORD chassis together. The unused address line outputs are pulled high (inactive) to comply with Dataram's addressing requirements.
The Raster Read Sequence Control block executes three data retrieval subcycles for each horizontal line, one for each channel. For each subcycle, this block determines the number of required WIDE WORDs. It executes a Sequential Read cycle to retrieve each channel's WIDE WORDs. The number of WIDE WORDs for each channel is a function of the zoom factor and the pixel starting address.

With a zoom factor of zero, it takes 40 WIDE WORDs to display a line. If the pixel start address is other than zero (due to roaming), an extra WIDE WORD is required (41 total). If the zoom factor is 15, two and one-half words are required. Thus, three words must be read. If the pixel start address is greater than 7 (due to roaming), an extra word is required (4 total). Using the zoom factor and pixel starting address, the Raster Read Sequence Control block determines the number of WIDE WORDs required for each channel. This function is performed by a PROM lookup table.

An integral part of the Raster Read Sequence Control block is the Read Control Interface. This block links the A Board to the Dataram WSC control board and accomplishes the following:

- sets the Dataram WIDE WORD memory mode to Sequential Read
- monitors the memory for initialization, busy and clear cycles
- completes the interlocked handshake control scheme between the A Board and the WIDE WORD Memory System

A Raster Read Sequence Control cycle consists of fetching Channel C's data, followed by fetching Channel B's data and completed by fetching Channel A's data. This cycle is executed once each horizontal scan (about 31 usec). The complete cycle is composed of three identical data fetching subcycles, each based on Dataram's Sequential Read cycle. This cycle is shown in Figure 14 below.

<table>
<thead>
<tr>
<th>Sync (480 nsec)</th>
<th>Sequential Read (120 N * nsec)</th>
<th>Sequential Halt (480 nsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>* N = number of WIDE WORDs read</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 14. Sequential Read Cycle
Figure 15. Raster Read Sequential Control Block Diagram
Timing of each phase of the Sequential Read cycle is accomplished by counting 40 nsec pixel clock pulses. The Sync and Sequential Halt phases require 12 clock pulses each. The Sequential Read phase requires 3 clock pulses per WIDE WORD. This phase ranges from 360 nsec to 4.92 usec (3 to 41 WIDE WORDs, respectively).

The Raster Read Sequence Control block consists of the following:

- Sequence Cycle Length Counter
- Number of WIDE WORDs Lookup
- Number of WIDE WORDs Counter
- Channel Counter
- Read Control Interface
- WIDE WORD Handshake Control
- Sequence Control Logic
- Double Strobe Generator
- Read FIFO Load Decode
- Zoom Factor Load Decode

Each of these blocks is described below and shown in Figure 15 on the adjacent page.

**Number of WIDE WORDs Lookup**

The Number of WIDE WORDs Lookup block, consisting of a PROM, determines the number of WIDE WORDs that must be fetched for each channel. The number of WIDE WORDs for each modulo 16 pixel start address (Read Address) and zoom factor combination is computed and stored in the PROM. This PROM is addressed by bits 0-3 of the Read Address (pixel start address) and the zoom factor. Its output represents the number of WIDE WORDs required.
Number of WIDE WORDs Counter

The Number of WIDE WORDs Counter is preset with the number of WIDE WORDs prior to the beginning of a channel's subcycle. The counter is set to the down count mode. The Sequence Control Logic block inhibits counting until the Sequential Read phase begins. See Figure 14 on page 4-43. During the Sequential Read phase, the Sequence Cycle Length Counter decrements the Number of WIDE WORDs Counter each time the Sequence Cycle Length Counter is preloaded (every three clock pulses). Upon reaching zero, the Number of WIDE WORDs Counter causes the Sequence Control Logic block to terminate the Sequential Read phase and begin the Sequential Halt phase. Therefore, the initial count loaded into the Number of WIDE WORDs Counter determines the number of 120 nsec Sequential Read cycles that are executed (3-41).

Sequence Cycle Length Counter

The Sequence Cycle Length Counter, clocked by pixel clock, times each phase of the Sequential Read cycle. The counter is controlled by the Sequence Control Logic.

Channel Counter

The Channel Counter is a down counter that is set to two prior to the beginning of the Raster Read Sequence Control cycle. Upon completion of a channel subcycle, the counter is decremented. Upon decrementing from zero to a minus 1, the counter generates an underflow which is used by the Sequence Control Logic to terminate the Raster Read Sequence Control cycle. The cycle (including the Channel Counter) is initialized at the beginning of the next horizontal line. The Raster Read Sequence Control Channel Mapping is shown in Table 8 below.

<table>
<thead>
<tr>
<th>Counter Output (Dec)</th>
<th>Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>A</td>
</tr>
</tbody>
</table>

Table 8. Raster Read Sequence Control Channel Mapping

The channel count is applied to the Zoom Factor Load Decoder and the Read FIFO Load Decoder. The Read FIFO Load Decoder block produces channel specific load strobes that latch WIDE WORD data into Channel A, B and C FIFOs. The Double Strobe Generator converts the Data Acknowledge signal from a single to a double strobe. Because the channel FIFOs are only 8 bytes wide (64-bits), two strobes are required to latch each WIDE WORD. The lower 64-bit word is latched first, followed by the upper 64-bit word. The Zoom Factor Load Decoder block produces channel specific load strobes that latch zoom factors into the Pixel Selector blocks.
The Read Control Interface consists of the WW Handshake CTL and part of the Sequence Control Logic block.

**WIDE WORD Handshake Control**

The WW Handshake CTL block deals with four interlocked handshake control signals:

- Address Available (output to the WIDE WORD memory)
- Address Acknowledge (input from the WIDE WORD memory)
- Data Request (output to the WIDE WORD memory)
- Data Acknowledge (input from the WIDE WORD memory)

Address Available is asserted at the beginning of each channel's Sync phase and remains asserted until the memory responds with the Address Acknowledge signal. Once the Sync phase completes, the Sequential Read phase is entered. Here, a read cycle begins by asserting Data Request. When the memory has the data on its output data bus, it asserts Data Acknowledge. On the A Board, the Data Acknowledge clears the Data Request. It is also used as a strobe for the WIDE WORD Data Latches block (see Figure 6, Sheet 1 on page 4-13) and a clock for the Double Strobe Generator.

**Sequence Control Logic**

The remainder of the Read Control Interface block consists of part of the Sequence Control block. This logic:

- sets the Sequential Read Mode for the WIDE WORD memory
- enables the address output of the Raster Read Address Generator (Read Address Enable in Figure 15)
- signals the end of each channel's Sequential Read phase (Read Done in Figure 15)

In addition, the Sequence Control Logic controls the counting and loading of the following counters:

- Number of WIDE WORDs Counter
- Channel Counter
- Sequence Cycle Length Counter
Double Strobe Generator

The Double Strobe Generator produces two read strobes each time Data Acknowledge is asserted. Data Acknowledge clocks the WIDE WORD Data Latches and the Double Strobe Generator. The two outputs of the Double Strobe Generator are labeled UWS and LWS (Upper Word Strobe and Lower Word Strobe, respectively). These strobes enable the output of the WIDE WORD Data Latches (described below).

Read FIFO Load Decoder

The Read FIFO Load Decoder block generates two channel FIFO load strobes for the channel specified by the Channel Counter block. The first load strobe stores the lower word output of the WIDE WORD Data Latches; the second load strobe stores the upper word output. This block gates the double strobe output of the Double Strobe Generator with the Channel Counter output to determine which set of Data FIFOs will receive load strobes.

Zoom Factor Load Decoder

The Zoom Factor Load Decoder generates a zoom load strobe for each channel's Pixel Selector block. Generation of these strobes is similar to the generation of the Read FIFO Load Decoder strobes. The difference is the strobe inputs. The Zoom Load strobe is asserted only while the start address for a frame or panel is being loaded. It is only at this time that data on the Zoom Factor bus (ZF0-ZF3) is valid. The output of the Zoom Factor Load Decoder latches the current channel's zoom factor into a latch within the channel's Pixel Selector block.

WIDE WORD Data Latches

Refer to Figure 6 on pages 4-13 and 4-14. WIDE WORD data from the memory is latched in the WIDE WORD Data Latches. This block consists of 16, 8-bit D-type latches. All 128 bits are latched simultaneously by the WIDE WORD Latch Strobe. However, data is output from these latches as two 64-bit words referred to as the lower and upper words. The lower and upper words are enabled onto the 64-bit MD bus by the Lower and Upper Word Strobes (LWS and UWS), respectively. The WIDE WORD is divided into two 64-bit words because each Channel's FIFO is 64 bits wide. By making these FIFOs 64 bits wide, the total chip count of the Channel A, B and C FIFOs is reduced by 50%. However, each channel must receive two load strobes, one for storing the lower word and another for storing the upper word. That is why the Double Strobe Generator is required.
The Channel A, B and C FIFOs store their respective WIDE WORDs as two 64-bit words. Each of these blocks consists of eight 8-bit FIFOs that, from an input perspective, appear as a single 512-word by 64-bit FIFO. That is, the Write Strobes of all eight FIFOs are parallel driven by the respective FIFO Load Strobe.

The read strobe for each FIFO within a channel is driven separately by eight read strobe outputs from the respective Pixel Selector block. These strobes sequentially read the eight FIFOs at the pixel clock rate. Each complete cycle of the Pixel Selector results in eight output bytes (pixels). Thus, two complete cycles of the Pixel Selector unload one WIDE WORD. From this point on, the channels are no longer referred to as A, B and C. These names are remapped to Channels 0, 1 and 2, respectively. Channel 0, Channel 1 and Channel 2 are also called the Graphics Channel, Image Channel 1 and Image Channel 2, respectively.

The Pixel Selectors control the data readout of their respective Channel FIFOs. FIFO characteristics and the roam and zoom features complicate this block. The effects of each of these are discussed individually below before analyzing the functional block diagram for the Pixel Selectors.

FIFOs are especially attractive in sequential storage and retrieval applications. However, when blocks of usable data are separated by blocks of unusable data, as occurs in the workstation during roaming, a flushing capability is necessary to flush the unwanted data. Flushing is required because entire WIDE WORDs (16 pixels) must be read from memory and stored in the Channel FIFOs when only part of the first and last word in a horizontal line may be used. FIFOs have no addressing capability. Therefore, if unwanted data is sandwiched between blocks of desired data, you cannot merely reindex an address pointer. You must provide a readout of each unwanted byte, thereby gaining access to the next usable data.

Roaming changes the pixel start address. If the pixel start address is non-modulo 16 (the first pixel displayed does not coincide with the first byte of the first word in a horizontal line), a synchronizer is required to read the unwanted bytes and stop when the byte representing the first display pixel is reached. Usually, non-modulo 16 pixel start addresses also result in unused pixels in the last word of a line. These pixels must be read out at the end of the line but they are not displayed.
Figure 16. Pixel Selector Functional Block Diagram
Zooming results in pixel replication. For example, if the magnification factor is 10 (zoom factor is 9), instead of displaying 640 different pixels in each horizontal line, 64 different pixels are displayed ten times each. Since each WIDE WORD contains 16 pixels, only four WIDE WORDs (five if roaming) are required to display a horizontal line. Thus, the zoom factor determines the rate of pixel reading.

Refer to Figure 16 on the adjacent page. As stated previously, each channel may have two sets of starting addresses and zoom factors. One set is used for a full screen; two sets are used for split panel, one for the upper and one for the lower horizontal panel. The Zoom FIFO and Start Address FIFO blocks in Figure 16 store the zoom factor and pixel start address, respectively. The Horizontal Switch Line (HSL) strobe reads out the lower panel zoom factors and start addresses in the split panel mode.

The output of the Zoom FIFO preloads the Zoom Pixel Hold-off Counter (down counter) with the channel's zoom factor. This counter, via the Match Logic block, enables the Pixel Counter. When the Pixel Counter is under control of the Zoom Pixel Hold-off Counter, it must underflow (decrement to -1) to enable the Pixel Counter. Since the Zoom Pixel Hold-off Counter is clocked by pixel clock, its underflow output enables the Pixel Counter to increment every zoom factor plus one pixel periods.

By storing WIDE WORDs as two 64-bit words, only eight FIFOs are required per channel. A disadvantage of this approach is pixel ambiguity. For example, if you are reading FIFO 0, are you reading pixel 0 or pixel 8 of the current WIDE WORD? To eliminate ambiguity, the Pixel Counter is always incremented until its output address is zero after displaying the last pixel of a horizontal line.

At the beginning of a new horizontal line, if the Start Address FIFO's output is other than zero, the End/Start Pixel Comparison Logic block generates a no-match input to the Match Logic block. This causes the Match Logic block to enable the Pixel Counter, allowing it to increment until its address matches the output of the Start Address FIFO. If, for example, the Start Address FIFO has an output of 8 (1000B), the Pixel Counter is allowed to increment eight times. This generates eight FIFO Read Strobes, flushing the first eight pixels from the Channel FIFOs.
This synchronizing takes place before the first visible pixel is displayed. Once synchronized, the FIFO Read Strobe Decoder block automatically maintains synchronism, generating two complete sets of FIFO Read Strobes (eight strobes per set) for each WIDE WORD. During roaming and zooming, it is probable that only part of the last WIDE WORD will be used. Regardless of how much of this word is displayed, all of it must be read out so you can gain access to the beginning of the next WIDE WORD (start of the next horizontal line).

The End/Start Pixel Comparison Logic detects the start of each WIDE WORD by comparing the FIFO 0 Read Strobe and the Pixel Counter's MSB. If both signals are low upon completion of the 640th visible pixel, the final WIDE WORD was completely used and no flushing is required. If these signals are unequal, the End/Start Pixel Comparison Logic sends a signal to the Match Logic block that enables the Pixel Counter. The Pixel Counter counts until the end of the current WIDE WORD is reached.

The Match Logic block multiplexes control signals from the Zoom Pixel Counter and the End/Start Pixel Comparison blocks to the Pixel Counter's Enable. During the horizontal blanking times (nonvisible pixels), the output of the End/Start Pixel Comparison block drives the Pixel Counter's count Enable input. During the visible pixel period, the Zoom Pixel Counter drives the Pixel Counter's Count enable input.
Screen Control Section

The Screen Control section shown in Figure 5 (page 4-4) consists of the following blocks in Figure 6 (pages 4-13 and 4-14).

- Horizontal and Vertical Panel Switch Generators
- Display Control

The Dual Channel can be partitioned into one panel (full screen), two panels (a left and right or top and bottom) or four panels (top, bottom, left and right). The Horizontal and Vertical Switch Generators generate the switch points. These switch points are inputs to the Display Control which generates three screen control signals (I1, I2 and W) that, at any instant, define which input channel (Image Channel 1, Image Channel 2 or the Graphics Channel) is driving the Dual Channel panel currently being scanned. I1, I2 or W is asserted when Image Channel 1, Image Channel 2 or the Graphics Channel, respectively, is driving the Dual Channel.

Horizontal and Vertical Switch Generators

Refer to Figure 17, the Panel Switch Generator and Display Control Functional Block Diagram, on the next page. Horizontal switch points are determined by counting pixel clock pulses; vertical switch points are determined by counting horizontal scan lines. Each generator consists of a memory mapped latch and a presettable down counter. The user defines each switch point (thus, the panel sizes) by writing to the respective latch. Each latch's output is used to preset a down counter. When the respective counter decrements to zero, the switch point is reached. The underflow from each counter is an input to the Vertical and Horizontal Switch Decode block. In addition, the Vertical Panel Switch Generator provides a binary count input to the Label Start Decode block.

The Label Start Decode block determines the beginning line of the upper panel's label field. Remember that the full screen/bottom panel label field is identified by logic in the Raster Read Timing section since it always starts on the ninth-from-the-last visible line. The upper panel label start is identified when the Vertical Panel Switch Generator has counted down to eight. At this time, nine lines (8-0) remain in the upper panel. Thus, regardless of the size of the upper panel, the label field will always be the last nine lines of the panel.
Figure 17. Panel Switch Generator and Display Control Functional Block Diagram
Display Control

The Control Word Latch is a memory mapped 16-bit latch. It is latched by PMSL (Panel/Mask Select Load - address 00000E00H) and latches the 16 LSBs of the FD (FIFOed Data) bus. The output of this latch is grouped into these four types of control signals:

- display mode controls (bits C, D and E)
- image panel masks (bits 0 - 7)
- graphics panel masks (bits 8, 9 and A)
- Window Cursor 2 control (bit F)

Three bits from the Control Word Latch define the display modes. These bits are inputs to the Channel Control logic. Table 9 defines the modes.

<table>
<thead>
<tr>
<th>Control Word EDC</th>
<th>Mode Code</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>0</td>
<td>Panels Off</td>
</tr>
<tr>
<td>0 0 1</td>
<td>1</td>
<td>Vertical Panels</td>
</tr>
<tr>
<td>0 1 0</td>
<td>2</td>
<td>Horizontal Panels</td>
</tr>
<tr>
<td>0 1 1</td>
<td>3</td>
<td>Quad Panels</td>
</tr>
<tr>
<td>1 0 0</td>
<td>4</td>
<td>Alternate Frame Stereo</td>
</tr>
<tr>
<td>1 0 1</td>
<td>5</td>
<td>Split Alternate Frame Stereo</td>
</tr>
<tr>
<td>1 1 0</td>
<td>6</td>
<td>Three Video Channels</td>
</tr>
<tr>
<td>1 1 1</td>
<td>7</td>
<td>Split Three Video Channels</td>
</tr>
</tbody>
</table>

Table 9. Display Modes

Twelve of the Control Latch outputs are used as image and graphics panel masks. Four bits are used for each channel. These bits define the panel that the respective channel is directed to.

The Window Cursor 2 Enable is a single-bit output of the Control Latch. It is used by the Prioritizer to enable the Window Cursor 2 feature.

The Vertical and Horizontal Switch Decode block uses switch points from the Vertical and Horizontal Panel Switch Generator to generate these switch signals:

- DTB (Delayed Top/Bottom)
- HSL (Horizontal Switch Line)
- TBG (Top/Bottom Gate)

DTB is low during full screen or upper panel scanning; it is high during lower panel scanning. This signal is used as an address input by the Label Generator and the File Address Multiplexer.
HSL is asserted only during the horizontal switch line. It is used by the Pixel Selectors and the Raster Read Address Generator. It disables the Raster Read Address Generator and enables the Raster Read Start Address Files (reads the start address for the lower panel).

TBG is used by the Video Blanking Generator and the Channel Control block which generates the I1, I2 and W screen control signals. The Control Word Latch, via its Mode and Mask inputs to the Channel Control block, provides channel-to-panel target information to the Channel Control block. The Channel Control block uses TBG and LRS (Left/Right Switch) to determine which panel is currently being scanned. The Mode and Mask information is used to determine which input channel is targeted for this panel. The I1, I2 and W signal outputs are processed by the Prioritizer into channel output multiplexer enable signals. Table 10 defines the screen controls.

<table>
<thead>
<tr>
<th>I1</th>
<th>I2</th>
<th>W</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No image or graphics</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Graphics</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Image Channel 2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Image Channel 1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Dual Channel</td>
</tr>
</tbody>
</table>

Table 10. Screen Controls

The Delay block in Figure 17 resynchronizes the switch points of the screen controls with the panel switch points by compensating for differences in propagation time (delays the screen controls one pixel clock period).
Prioritizer

Figure 18 on the next page is the Prioritizer Functional Block Diagram. The Prioritizer assigns a priority to all data sources capable of writing to any output channel. Priority control is accomplished by manipulation of the channel multiplexer enable signals. The data source priorities are:

- label characters (highest)
- label field
- graphics
- image (lowest)

The graphics inputs to the Prioritizer are via two NOR gates. The lower gate produces a low output if any of its inputs are high (bits 0-3); the upper gate produces a low output if any of its inputs are high (bits 4-7). The graphics inputs are split into two halves to allow four graphics bit planes for each image channel during stereo display. Image Channel 1 graphics bits are loaded into bit planes 0 - 3; Image Channel 2 graphics bits are loaded into bit planes 4 - 7.

Cursor inputs (CUR0 and CUR1) cause the Prioritizer to enable the Graphics Channel input to the Dual Channel Multiplexer. The only way to pass cursor bits to the Dual Channel is through the Graphics Channel.

I1, I2 and W are the screen control signals that identify the data source for the panel currently being scanned. These signals are described on page 4-55.

MC0 and MC1 are processed mode control outputs of the Channel Control block of the Panel Switch Control section. The Channel Control block compresses the eight mode input codes to four output codes. Table 11 shows the compression.

<table>
<thead>
<tr>
<th>Mode Input</th>
<th>MC1</th>
<th>MC0</th>
<th>Output Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 11. Mode Compression
Figure 18. Prioritizer Functional Block Diagram
Mode compression is possible because paneling and data source information is provided by the screen control signals (I1, I2 and W). MC0 and MC1 control Image 1 and 2 Multiplexer outputs and the Dual Channel's Multiplexer output. I1, I2 and W are used by the Dual Channel only.

Latched CHGN (Latched Character Generator output) provides the Prioritizer with label pixel information. When this signal is asserted, the Label Generator is currently writing a label pixel.

The MSB output of the Control Word Latch (shown in Figure 17) is called Window Cursor. It is an input to the Delay block in Figure 18 and functions as an enable for the Window Cursor 2 feature. When Window Cursor is asserted and a pixel within the Cursor 1 box defined by its position, height and width parameters is scanned, the inputs to the Delay block are qualified. The Delay block's output is asserted one pixel clock period later (delayed one clock pulse), enabling the Window Cursor input to the Prioritizer. When the Window Cursor input is enabled, the Image Channel 1 and Dual Channel inputs to the Dual Channel Multiplexer are disabled, and the Image Channel 2 input is enabled, displaying Image Channel 2 in the Cursor 1 field.

Label Background is the second highest data priority. The Label Background Blank Logic PAL block combines a label field output signal from the Label Generator with a channel mask output of the Mask Latches (see sheet 2 of Figure 6 on page 4-14). The Mask Latches provide Label Generator channel assignment to the Label Background Blank Logic PAL which provides three control inputs to the Prioritizer: an Image Channel 1 label field, an Image Channel 2 label field and a Graphics Channel label field. Whenever the Label Generator is active, one of these signals is asserted regardless of whether the pixel being scanned is a background or label pixel. The Prioritizer determines whether the pixel is a background pixel or label pixel by examining Latched CHGN when one of the control inputs from the Label Background Blank Logic PAL is asserted.
Lookup Tables Section

The Lookup Tables were first introduced in Figure 5 and described in the WIDE WORD A Board Simplified Functional Description. The Lookup Tables in Figure 5 consist of sheet 2 of Figure 6. Data inputs to this section are:

- Channel A, B and C FIFO outputs (V0B0-7, V1B0-7 and V2B0-7, respectively)
- Cursor 0 bit (CUR0)
- Cursor 1 bit (CUR1)
- Character Generator bit (CHGN)
- Channel Palette programming

Control inputs to this section consist of:

- Prioritizer controls
- Graphics Label Background
- data masks
- blanking masks
- panel switching
- blink control
- TV timing signals

The Lookup Tables section consists of these five digital processing channels:

- Graphics Channel
- Image Channel 1
- Image Channel 2
- Dual Channel
- Interlaced Dual Channel

The Dual Channel is formed from inputs from Image Channels 1 and 2. The Graphics Channel is multiplexed into Image Channel 1, Image Channel 2 and the Dual Channel. It does not have a dedicated analog output channel. A fourth output channel converts the Dual Channel's output to the interlaced RGB (Red, Green, Blue) format for viewing on a standard RGB monitor. The final stage of each channel contains a D to A converter that produces analog RGB drives.
Graphics Channel and Image Channels 1 and 2

Image Channels 1 and 2 are identical. The Graphics Channel is identical to the Image Channels up to the output multiplexers. Therefore, this section describes Image Channel 1 in detail. The Graphics Channel and Image Channel 2 are described by noting differences. The Dual Channel and Interlaced Dual Channel are described separately.

Channel Data Latches

The 8-bit output of the Channel B FIFO is latched in the Image 1 DataLatch. The latch, clocked by pixel clock, resynchronizes the output of the Channel B FIFO with the pixel clock.

The Channel 1 DataLatch outputs its data to the Image 1 and Dual Channel Mask Gates. The Dual Channel Mask Gates are actually the beginning of the Dual Channel. Refer to the Dual Channel Description on page 4-68 for additional information.

Cursor/Blink/Character Latch

The Cursor/Blink/Character Latch latches the outputs of the:

- Cursor 0 Generator (CUR0)
- Cursor 1 Generator (CUR1)
- Blink Generator (BINK)
- Character Generator (CHGN)

The four output bits of this latch are applied to the Graphics, Image 1 and Image 2 Mask Gates. Thus, including the outputs of the respective Channel DataLatch, each of these channels has 12 data input bits.

Channel Mask Latches

The Channel Mask blocks any or all of the 12 data bits from continuing through the channel.

The 16-bit memory mapped Image 1 Mask Latch is loaded from the FD bus during the vertical blanking period. The eight LSBs (bits 0-7) of the mask's output correspond to the eight Image 1 Data Latch output bits (V10-V17). The next four bits (8-11) mask Cursor 0, Cursor 1, the Label Generator, and the Blink Generator outputs. The last four bits (12-15) are inputs to the Video Blanking Generator.
Video Blanking Generator

The Video Blanking Generator blanks panels or full screens of Image 1, Image 2, the Dual Channel and/or the Graphics Channel. The generator provides three outputs: VB1 and VB2 (Video Blanking 1 and 2, respectively) to the Image 1, Image 2 and Dual Channel Mask Gates, and VBG (Video Blanking Graphics) to the Graphics Mask Gates.

Blanking for each channel is defined by the four MSBs of each channel's 16-bit mask word. The four Video Blanking Generator bits define blanking for a panel or full screen. These bits do not affect the Cursor, Label or Blink data bits. The four blanking bits can specify video blanking for:

- a full screen
- an upper horizontal panel
- a lower horizontal panel
- a left vertical panel
- a right vertical panel

Channel Mask Gates

The Image 1 Mask Gates can block any data bit output of the Channel 1 Data Latch and/or any output of the Cursor/Blink/Character Generator. It allows the user to blank the channel for the entire screen, or a vertical or horizontal panel.

The Image 1 Mask Gates consist of twelve AND gates, one for each Image 1 Data Bit and one for each output of the Cursor/Blink/Character Latch. Each of the eight data bits from the Channel 1 Data Latch is applied to a 3-input AND gate. The other two inputs for each gate are the Image 1 Mask Latch and VB1 (Video Blanking 1). Thus, any of the eight data bits are blocked when their respective mask is low, and all eight data bits are blocked when VB1 is low. Each of the four outputs of the Cursor/Blink/Character Latch is applied to 2-input AND gates along with a corresponding mask bit from the Image 1 Mask Latch. Thus, these bits are blocked (masked off) only if their respective mask bit is low.

Masking is especially useful in Graphics Channel control. Since each graph overlay occupies a bit plane, an entire graph can be enabled or disabled by a single mask bit. Masking is also useful for image channel processing. Here, the 8-bit channel data represents satellite sensor magnitudes. A specific range of magnitudes may be passed or blocked using the mask gates. For example, infrared (IR) sensor data directly relates to temperature and altitude (higher cloud formations are colder). If the user wants to remove the low cloud components of the IR image, the six or seven LSBs of the incoming data could be masked off, allowing only the highest magnitude data to be displayed. The Image 1 Mask Gates drives the Masked Image 1 Latch.
Masked Channel Latches

The Image 1 Mask Gates drive the inputs of the Masked Image 1 Latch. This latch resynchronizes the outputs of the Image 1 Mask Gates to pixel clock. It is also part of a multiplexer consisting of the Masked Image 1 Latch and the Image 1 Palette Load Address Buffers. While painting visible pixels, the Masked Image 1 Latch is enabled; during vertical blanking, the Image 1 Palette Load Address Buffers are enabled, allowing the PS/2 to program the Image 1 Palette RAM.

Channel Palette RAMs

The Image 1 Palette RAM provides pseudocoloring to Channel 1 images. It is organized as a 4K by 24-bit RAM and drives the red, green and blue 8-bit buses.

The RAM's 12 address lines are driven by the outputs of the Masked Image 1 Latch. Thus, its address lines are driven by the eight bits of Image 1 data plus the four outputs of the Cursor/Blink/Character Generator. By assigning values of Red, Green and Blue (RGB) for each possible data combination (12 bits result in 4,096 unique combinations), a specific color and brightness can be assigned to:

- each Image 1 data value (0-255)
- Cursor 0
- Cursor 1
- label characters
- each of the above with and without Blink asserted

The Palette RAM consists of 16, 256-word palettes. Selecting a palette is accomplished by the 4-bit output of the Cursor/Blink/Character Generator. Table 12 on the adjacent page shows the lookup palettes.

Palette 0 assigns a color to each Image 1 data value. For the Graphics Palette RAM, address 0 of Palette 0 defines the Image 1 and 2 label background colors. The Prioritizer enables the output of the Graphics Palette RAM into the respective Channel DAC during image label fields, except while painting a character pixel. It switches back to the respective channel while painting a character pixel. At present, label characters come from the Graphics Channel Palette RAM.
## Table 12. Image 1 Palette RAM Map

<table>
<thead>
<tr>
<th>Palette Number</th>
<th>Address (Hex)</th>
<th>I1BINK</th>
<th>I1CHGN</th>
<th>I1CUR1</th>
<th>I1CUR0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00-FF</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Data Coloring</td>
</tr>
<tr>
<td>1</td>
<td>100-1FF</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Cursor 0 Coloring</td>
</tr>
<tr>
<td>2</td>
<td>200-2FF</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Cursor 1 Coloring</td>
</tr>
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<td>3</td>
<td>300-3FF</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Merged Cursor Coloring</td>
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<td>4</td>
<td>400-4FF</td>
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<td>Character Coloring</td>
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<td>8</td>
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<td>Data Coloring during Blink</td>
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*Revised 10/92*
Providing BINK is not asserted and there are no active graphics or cursor bits, address 0 of the Graphics Palette RAM supplies the image label background color. If either cursor, a graphics bit or BINK is active and masked on via the Graphics Mask Gates while painting image label background pixels, the image label background color is replaced by the color assigned to the respective enhancement. Thus, in a horizontal split screen showing two images on the Channel 1 or Channel 2 monitor, graphics may appear in the split screen label. If the cursor is enabled into the Graphics Channel, it appears in the image label background as the cursor moves through the split screen label. If the cursor is enabled to the respective image channel only, it goes behind the split screen label as it moves through the label.

Palettes 1 and 2 assign a color value to Cursor 0 and Cursor 1, respectively. Palette 3 assigns a color to pixels that are part of both cursors (one cursor is moved through the other). In Palettes 1, 2 and 3, each of the 256 addresses should be set to the same value. Palette 4 assigns a color value to the active label characters. All 256 of its addresses should be set to the same value. Since each channel has its own Palette RAM, each channel's label can be a different color.

Palettes 5 and 6 are for character labels in combination with Cursors 0 and 1, respectively. Palette 7 assigns a color to pixels that are part of both cursors and a label character. Palettes 8-15 are the blink (BINK asserted) counterparts of Palettes 0-7, respectively. When blink is enabled, most of the blink palettes will be identical to their nonblink counterparts. Usually only one or two palettes will be altered to enhance a particular aspect of the display. For example, changing the image data palette above a specified magnitude threshold can be used to flash alternate colors for severe storms, etc.

Channel Multiplexer

The RGB output of the Image 1 Palette RAM is applied to a set of tri-state D-type latches. The RGB output of the Graphics Channel is applied to a second set of tri-state D-type latches. These two sets of latches make up the Channel 1 Multiplexer. A similar arrangement makes up the Channel 2 Multiplexer (Graphics and Image Channel 2). The multiplexer selects either image or graphics data to be displayed. Multiplexer data selection is controlled by the Prioritizer.

Channel DACs and Sync Driver

The 24-line RGB output of the Channel 1 Multiplexer drives the Channel 1 DAC (Digital to Analog Converter). The 24-line input consists of eight lines each for red, green and blue. The Channel 1 DAC converts each 8-line input to an analog value and outputs this voltage to a 75-ohm coaxial ribbon cable. The Channel 1 DAC's RGB analog output drives a non-interlaced RGB monitor. The monitor also requires a composite sync signal. The Sync Driver amplifies the composite sync output of the Raster Read Timing block and impedance matches it to the coaxial cable and monitor.
When the optional WIDE WORD Interlace Adapter Board is mounted on the A Board, the Channel 1 DAC, Channel 2 DAC and Sync Driver chips are removed and their IC sockets function as connectors J1, J2 and J4, respectively. By using these sockets as connectors, the adapter board gains access to data and control signals needed for generating the interlaced Image Channel 1 and Image Channel 2 outputs. Refer to the Interlaced Dual Channel description for more information.

**Dual Channel**

Infrared (IR) images show cloud height as a function of temperature; visible images show clouds as a reflection of sunlight. Often, it is desirable to enhance visible images using cloud height pseudocoloring. When IR and visible images are obtained at the same time for the same location, they can be displayed simultaneously via the Dual Channel. Visible data is processed by one image channel; IR data is processed by the other. By assigning appropriate colors to the various IR intensities, the visible image appears to be overlaid with the color enhanced IR data. This type of display is called a Nortlie function or display. The Dual Channel can also be used as a single 16-bit display.

From a hardware perspective, the Dual Channel begins with the Dual Channel Mask Gates and Dual Channel Mask Latch. The eight Image 1 data bits form the lower half of the Dual Channel data bus; the eight Image 2 data bits form the upper half. This bus drives the Dual Channel Mask Gates. The Dual Channel Mask Latch is a memory mapped latch that allows the user to select which data bits will pass through the Dual Channel Mask Gates. VB1 and VB2 are also applied to the Dual Channel Mask Gates. VB1, when low, blocks the Image 1 input; VB2, when low, blocks the Image 2 input.

**Masked Dual Channel Latch**

The Masked Dual Channel Latch resynchronizes the 16-bit output of the Dual Channel Mask Gates and forms part of an address multiplexer for the Dual Channel Palette RAM. Data is latched on the rising edge of pixel clock. The latch's output data is enabled to the Dual Channel Palette RAM during display of the visible horizontal lines (DVG/ - Delayed Vertical Gate is asserted).
The Dual Channel Palette Load Address Buffers form the other part of the Dual Channel Palette RAM address multiplexer. They allow the PS/2 to address the Dual Channel Palette RAM (via the B Board) during palette loading. This portion of the multiplexer is enabled only during the blanked horizontal lines (vertical blanking period) by DVG (Delayed Vertical Gate). Since DVG is an inversion of DVG/which enables the Masked Dual Channel Latch's output, only one address source (PS/2 or the Dual Channel Mask Gates) drives the Dual Channel Palette RAM at a time.

The Dual Channel Palette RAM is similar in function to the other Palette RAMs. The main difference is its size. Since the Dual Channel Palette's address bus is driven by the 16 Image 1 and 2 data bits, the palette has a 64K addressing range. Each location is 24 bits wide to accommodate eight bits for each output color magnitude (red, green, and blue). Thus, the RAM is organized as 64K by 24 bits.

With the exception of the Dual Channel Palette RAM, all A Board memory mapped registers and RAMs are rewritten every vertical blanking period. About 16 vertical blanking periods are required to rewrite the Dual Channel Palette.

The Dual Channel Multiplexer allows one of these four signal sources to drive the Dual Channel DAC:

- Image 1
- Image 2
- Dual Channel (Image 1 plus Image 2)
- Graphics

Signal source selection is accomplished by the Prioritizer.

The Dual Channel Multiplexer consists of four sets of 24-bit tri-state latches that are clocked by pixel clock. Each latch set latches the 24 RGB bits of its respective palette RAM. The multiplexer's output also drives the Interlaced Dual Channel.

The 24-line RGB output of the Dual Channel Multiplexer drives the Dual Channel DAC. The RGB input has eight lines each for red, green and blue magnitudes. The DAC converts each 8-line input to an analog voltage and outputs this voltage to a 75-ohm coaxial ribbon cable. The RGB analog output drives a non-interlaced RGB monitor. An additional input requirement of the monitor is a composite sync signal. The Sync Driver amplifies the composite sync output of the Raster Read Timing block and impedance matches it to the coaxial cable and monitor.
Interlaced Dual Channel

Two Dual Channel frames are written in the period of time specified for one interlaced TV frame. One frame pair, consisting of two non-interlaced Dual Channel frames, produces one interlaced frame. During the first non-interlaced frame (called the even frame), 263 even numbered lines are extracted to produce the 262-1/2 line even field. Then, the 262 odd numbered lines of the next non-interlaced frame (odd frame) plus the unused half line from the first frame are used to produce the 262-1/2 line odd field.

Alternate Line Gate

The Alternate Line Gate generates write strobes for the Interlace FIFOs (horizontal line buffer). It passes the 640 pixel clock pulses that correspond to the 640 visible pixels by gating pixel clock with Odd/Even Line (OEL) and Composite Blanking. Composite Blanking allows pixel clock pulses only during visible pixels. OEL toggles at the end of each horizontal line and gates off pixel clock pulses when it is low. OEL is high on the first line of the first frame (even frame) of each frame pair. Thereafter, for the next 1049 lines, it toggles. Write strobes are generated for visible pixels during every other horizontal line. This signal is passed to the optional WIDE WORD Interlace Adapter Board for the purpose of converting Image Channel 1 and Image Channel 2 to interlaced format.

Pixel Clock Divide-By-Two

Since the interlaced horizontal scan rate is one-half that of the non-interlaced display, data must be read from the Interlaced FIFOs at one-half the non-interlaced pixel clock rate. The Pixel Clock Divide-By-Two block produces Interlaced FIFO read and Interlaced Dual Channel DAC clock strobes by dividing the A Board’s pixel clock by two.

The Interlaced Dual Channel DAC requires a continuous clock signal; the Interlace FIFO requires read strobes only during the visible portion of the horizontal scan. Although these two signals are generated by separate dividers, they must be in phase with each other when both are present. This allows the FIFO output data to be latched into the DAC at the end of each read strobe (data has maximum stability at this time). To ensure synchronism between the strobes, the DAC clock generator receives a synchronizing input from the FIFO read strobe generator. This signal is passed to the optional WIDE WORD Interlace Adapter Board for the purpose of converting Image Channel 1 and Image Channel 2 to interlaced format.
Interlace FIFO

The Interlace FIFO is a dual ported line buffer. Data writing and reading may be performed asynchronously. Data is written under control of pixel clock and is read at pixel clock divided by two.

A complete 640-pixel line is written in slightly over 31 usec. During this time, half the pixels are output to the DAC. The next line is prevented from being written into the FIFO though reading continues. Thus, at the end of each two-line input pair, the FIFO is empty. The maximum number of pixels in the FIFO is 320 (640 pixels in minus 320 pixels out). This is why only a 512-word by 24-bit FIFO storage capacity is required.

Interlaced Dual Channel DAC

The Interlaced Dual Channel DAC is a triple 8-bit video DAC designed for high performance, high resolution color graphics. It converts the 8-bit RGB digital inputs into RS-343A compatible video signals and outputs these signals into a doubly-terminated, 75-ohm load. Interlaced Composite Sync, Interlaced Composite Blanking and the three 8-bit RGB inputs are latched into the DAC on the rising edge of the clock.

When the optional WIDE WORD Interlace Adapter Board is connected to the A Board, the Interlaced Dual Channel DAC is relocated to the optional board. The DAC's original IC socket functions as the J3 mating connector. Thus, the RGB input, the Interlaced Sync and the Interlaced Blanking signals are looped through the optional board, and the interlaced analog outputs are passed back to the A Board. The interlaced sync and blanking signals are used by the Channel 1 and Channel 2 interlace converters and the Interlaced Dual Channel DAC located on the optional board.

Interlaced Sync Driver

The Interlaced Sync Driver is identical in function to the Channel 1, Channel 2 and Dual Channel Sync Drivers. However, the input signal is different. The Interlaced Sync Driver is driven by Interlaced Sync. Equalization pulses are required for interlaced displays. The Interlaced Sync signal is generated by the Raster Read Timing section specifically to comply with the Interlaced Sync signal specifications.
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A Board Detailed Circuit Description

The schematic diagrams of the WIDE WORD A Board are shown on SSEC drawing 6450-0563 (Revision V6, dated 08/23/91). This Detailed Circuit Description discusses the logic of these blocks shown in the functional block diagram in Figure 6 on pages 4-13 and 4-14:

- Buffer and Decode Section
- Pixel Clock Generator
- Raster Read Timing Generator
- Cursor Generators
- Label Generator
- Blink Generator
- Raster Read Section
- Screen Control Section
- Prioritizer
- Lookup Tables Section

Schematic Conventions

The WIDE WORD A Board is built on a Dataram multilayer form factor board. Locations on the board are described by the row designator (X1-X60) and column designator (Y1-Y169). Each schematic circuit symbol is labeled by the XY coordinate of its pin 1 location. The Detailed Circuit Description that follows refers to ICs by this location label. A reference to a schematic circuit symbol of a multiple section device uses the symbol ID followed by a letter designator. The symbol ID alone refers to single function ICs.

Logic Conventions

Logic signals are indicated by all uppercase letters and numbers, e.g., FSHL. A logic signal name ending with a trailing slash represents an active low signal, e.g., RRS/.

Several conventions that can describe the state of a logic signal are: true or false, high or low, one or zero, and active or inactive. In the following description, all logic states are described as high and low. This convention best describes the physical condition of a logic signal and is better suited for troubleshooting.

Frequently, a logic signal is "asserted." If a signal with a trailing slash is asserted, it is low. If a signal without a trailing slash is asserted, it is high. Thus, asserted means that a signal is in its active state.
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Table 13. Memory Mapped Strobes (Numerical Order)
Buffer and Decode Section

Refer to Figure 6, the A Board Detailed Functional Block Diagram, on pages 4-13 and 4-14, and sheet 2 of the schematics.

AddressLatch

The B Board sends 18-bit addresses to the A Board. These address lines enter the A Board on the JB connector (JB01-JB18). The 10 LSBs of the address are latched into X57Y36; the 8 MSBs are latched into octal latch X53Y38. Though these latches are tri-state types, their outputs are always enabled because their tri-state inputs are grounded. The outputs of these latches (FA00-FA11) drive FIFOed Address lines 00-11H. These latches are latched by the rising edge of DLS (Data Latch Strobe) which is generated by the B Board and sent to the A Board on JA25. Refer to the B Board Detailed Circuit Description for additional information on DLS.

DataLatch

The B Board sends 24-bit data words to the A Board. These lines enter the A Board on the JA connector (JA01-JA24). The Data Latch section consists of three transparent D-type octal latches located at X57Y12, X57Y1 and X53Y1. These latches are strobed by DLS. Unlike the Address Latch, the Data Latch outputs follow the inputs while DLS is high. The Data Latch latches its inputs on the falling edge of DLS. Note that the Data Latch is unidirectional, i.e., there is no provision for sending A Board data back to the B Board or the PS/2. The output of the octal latches drive FD00-FD17 (FIFOed Data lines 00-17H).

Memory Mapped Control and Strobe Delay

The Memory Mapped Control decoder consists of three PALs located at X57Y23, X53Y12 and X53Y25. Each of these chips uses the upper 10 bits of the PA bus to decode 10 memory mapped strobes. Table 13 on the adjacent page shows the address to strobe mapping in increasing address order.
The Strobe Delay block shown in Figure 6 consists of two series connected buffers located at X39Y18A and X39Y18B. Together, these buffers provide about 10 nsec of propagation delay for DLS, the Strobe Delay input. DLSDD (Data Latch Strobe Double Delayed), the Strobe Delay output, allows the address inputs to the Memory Mapped Control PALs to stabilize (setup time) before enabling the strobe decode logic.

Pixel Clock Generator

Refer to sheet 34 of the schematics. Due to the large number of components that must be synchronized to pixel clock, a pixel clock generator having a large fan out is required. In addition, long clock runs experience unacceptable propagation delays. This is minimized by dividing the clock loads into seventeen short clock runs. Each run is driven by one section of a six-section low skew gallium arsenide technology clock buffer IC. These chips allow phase adjustment and control.

The 25.5454514 MHz crystal oscillator located at X51Y64 is buffered by the gallium arsenide clock buffer located at X53Y63. The grounded S0 and S1 programming inputs to this chip (pins 3 and 4, respectively) and the phase correcting feedback from the Q0 output (pin 10) cause the PXLCK1 through PXLCK5 drive outputs to be in phase with the oscillator output. PXLCK1 through PXLCK5 drive clock buffer chips X17Y54, X47Y82, X39Y123, X39Y114 and X53Y54, respectively.

Note that X17Y54, X39Y123 and X53Y54 are programmed the same as X53Y63 described in the preceding paragraph. These chips produce 14 clock signals that are in phase with each other and the input signals. Thus, these outputs are all in phase with the clock oscillator (X51Y64) output.

PXLCK-E, produced by X47Y82, leads the in-phase outputs by 6 nsec. PXLCK-K and -Q are produced by X39Y114. PXLCK-K and -Q lead the in-phase outputs by 6 and 2 nsec, respectively. This is a function of the S0 and S1 programming inputs and the selected output used for feedback. See Table 14 on the next page for output phase relationships.
X47Y82 has both programming inputs pulled high and uses Q1 and Q2 for feedback. This causes the Q5 input to lead the PXLCK2 input by 6 nsec. The remaining outputs of X47Y82 are unused. See Table 14 below output phase relationships with respect to the input.

Table 14 summarizes the clock driver programming.

<table>
<thead>
<tr>
<th>Select Pins</th>
<th>Output Fed To FBIN</th>
<th>Output Phase Shift (nanoseconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 S0</td>
<td>Q0</td>
<td>Q0 Q1 Q2 Q3 Q4 Q5</td>
</tr>
<tr>
<td>0 0</td>
<td>Q0</td>
<td>0 0 0 0 0 1*</td>
</tr>
<tr>
<td>1 0</td>
<td>Q1</td>
<td>-2 0 -2 -4 -6</td>
</tr>
<tr>
<td>1 1</td>
<td>Q1, Q2</td>
<td>-2 0 0 -4 -4 -6</td>
</tr>
</tbody>
</table>

* 1 = Inverted

Table 14. Clock Driver Programming

Raster Read Timing Generator

The Raster Read Timing Generator is shown on sheet 3 of the schematics. Also refer to Figure 7 on page 4-18 and the applicable PAL equations.

Horizontal Counter

The Horizontal Counter consists of X43Y60, an 8-bit up/down counter, and X43Y73, a 4-bit up/down counter. These counters are cascaded to function as a 10-bit up counter. They operate synchronously and are clocked by PXLCK-O. Both counters are preset to zero on the rising edge of PXLCK-O when HCR (Horizontal Count Reset) is low. HCR is described in the Horizontal Decode PAL description. After HCR returns high, X43Y60 increments on the rising edge of each PXLCK-O pulse. Upon reaching 255, X43Y60 drives its pin 14 low, enabling X43Y73. On the next clock pulse, X43Y73 increments to one and X43Y60 overflows to zero. At this time, X43Y73 is again disabled. This counting process continues until pins 13 and 14 of X43Y73 are high and X43Y60's pins 2, 3 and 5 are high (count = 779). When this count is reached, the Horizontal Decode PAL (PAL A3) asserts HCR, resetting X43Y60 and X43Y73 to zero.
Note that NAND gate X41Y18C drives the D-input of counter X43Y73. This input is not part of the Horizontal Counter. As described above, only the QA and QB sections (pins 14 and 13, respectively) are part of this counter. The QC section is not used and the QD section functions as a D-type latch for the output of NAND gate X41Y18C. This gate's output signal is latched on the rising edge of PXLCK-O when HCR/ is asserted (coincident with the rising trailing edge of HCR/).

Vertical Counter

The Vertical Counter consists of counters X43Y25 and X43Y38. Operation of this counter is similar to the Horizontal Counter. Note that the Vertical Counter is enabled only during the time HCR/ is low by applying HCR/ to X43Y25's pin 13 (CET - Count Enable T). Thus, this counter increments at the end of each horizontal line. X43Y12, the Vertical Decode PAL, and OR gate X45Y66D generate a VCR (Vertical Count Reset) when the cascaded count in X43Y25 and X43Y38 reaches 524D. The D-input of X43Y38 is used as a D-type latch that latches on the rising edge of PXLCK-O when VCR is low (end of each field).

Horizontal Decode PAL

The Horizontal Decode PAL is A3, a 22V10A PAL located at X43Y47. Refer to the A3 PAL equations located in the Reference section of this manual for more information.

LG/

LG/ (Line Gate) is high during the vertical blanking lines (lines 0 through 42) and during pixels 0-127 and 768-779 of horizontal lines 43-524. Thus, LG/ is low during pixels 128-767 (640 total) of lines 43-524 (482 total).

DLG/

DLG/ (Delayed Line Gate) is low during visible pixels only. This signal is nearly identical to LG/ except that DLG/ is high during lines 0-43, resulting in 481 visible lines (44-524).

SYNC/

SYNC/ is required by all output DACs except the Interlaced Dual Channel DAC. It consists of vertical and horizontal sync components. Refer to Timing Diagram 2 on the adjacent page.
The horizontal sync for the next line begins a few pixels before the current line ends. It consists of pixels 745-779 of the current line and pixels 0-31 of the next line (67 pixels total). The horizontal sync component is generated for all horizontal lines, including the 43 lines that occur during the vertical blanking period.

The vertical sync occurs during horizontal lines 6-11. Horizontal sync must be maintained through this period as well as indicate vertical sync. To accomplish this, the horizontal sync pulses are stretched an additional 627 pixels, making horizontal sync pulses for lines 6-11 694 pixels in duration. Thus, during this time, SYNC/ is high during pixels 659-744 (86 pixels total).

Refer to Timing Diagram 2. BLANK/ is the composite blanking signal required by all DACs except the NTSC DAC. In addition, the Alternate Line Gate logic (see sheet 2 of Figure 6 on page 4-14) uses BLANK/ to gate pixels into the Interlace FIFO. BLANK/ is low during horizontal lines 0-43 and during pixels 770-779 of the current line and pixels 0-130 of the next line (140 pixels total).

The NCS/ (NTSC Composite Sync) consists of horizontal and vertical sync components. The vertical sync component contains horizontal sync information because its duration spans three interlaced horizontal scan lines. Generation of NCS/ consists of dividing the desired output waveform into regions in which the sync characteristics are constant, implementing each of these regions in logic and combining the individual logic blocks to produce the composite signal.

The inputs to the logic blocks are the pixel count from X43Y60, OEL (Odd/Even Line) and V10, V11 and V12. V10, V11 and V12 separate the vertical blanking period into these three regions.

- V10 is asserted during horizontal lines 0-5, 12-17 and 43.
- V11 is asserted during horizontal lines 0-5 and 12-42.
- V12 is asserted during horizontal lines 6-11.

Timing Diagram 3 on page 5-7 shows the NCS/ waveform. Remember that two non-interlaced horizontal lines form one interlaced horizontal line. Except during the vertical blanking period, OEL inhibits all horizontal sync generation by the second horizontal line of each non-interlaced horizontal pair (OEL is low). During the vertical blanking period, both horizontal lines generate the serrated vertical sync pulse and the equalization pulses.
Timing Diagram 4. Vertical Timing
NCB/ (NTSC Composite Blanking) is shown in Timing Diagram 3 on page 5-7. The vertical blanking component begins 41 pixel clock periods before the beginning of a frame and extends through non-interlaced line 43. Thus, 44 non-interlaced horizontal lines are blanked during each interlaced vertical field. Since there are two vertical fields in each interlaced frame, 88 of the 1060 non-interlaced lines in each non-interlaced pair of frames are blanked, leaving 962 unblanked lines. Because only every other line is displayed, 481 interlaced lines are displayed in each interlaced frame.

Horizontal blanking begins 41 pixel clock periods before the beginning of a horizontal sync pulse and continues for 119 pixel clock periods after the end of the horizontal sync pulse. This results in 1280 unblanked pixel clock periods in each non-interlaced horizontal pair. Since two non-interlaced clock periods occur during each interlaced pixel period, the interlaced horizontal scan line is unblanked for 640 pixels.

HCR/ (Horizontal Count Reset) is asserted for one pixel clock period (about 40 nsec) when the count input from X43Y60 (8 LSBs) and X43Y73 (2 MSBs) reaches 779. HCR/ resets these two counters to zero, resulting in a count range of 0-779 (780 total). This count range defines the number of pixels and the scan period of a horizontal line.

Vertical Decode PAL

PAL A2A, located at X43Y12, is the Vertical Decode PAL. Refer to the PAL A2A equations in the Reference section of this manual for more information. Timing Diagram 4 on the adjacent page shows most of A2A’s output signals.

VI0 (A2A’s pin 15 Output) is used by A3 (Horizontal Decode PAL) only. This signal is asserted during horizontal lines 0-5, 12-17 and 43.

VI1 (A2A’s pin 16 Output) is used by A3 (Horizontal Decode PAL) only. This signal is asserted during horizontal lines 0-5 and 12-42.

VI2 (A2A’s pin 17 Output) is used by A3 (Horizontal Decode PAL). It is also available at the rear connector panel of the WIDE WORD chassis via inverting driver X33Y1F, line driver X51Y111A and pin 20 of the VP (Video Port) plug. This signal is asserted during horizontal lines 6-11 (horizontal drive time).
Timing Diagram 5. Odd/Even Line and Field Timing
VG and VG/ : VG and VG/ (Vertical Gate) complement each other. These signals are the outputs of X43Y12's pins 19 and 20, respectively. They are asserted during horizontal lines 0-42 and are used extensively throughout the A Board.

DVG and DVG/ : DVG and DVG/ (Delayed Vertical Gate) complement each other. These signals are the outputs of X43Y12's pins 21 and 22, respectively. They are similar to VG and VG/ above, except DVG and DVG/ extend one additional horizontal line. That is, they are asserted during horizontal lines 0-43.

LSL/ : LSL/ (Label Start Line) is asserted during horizontal line 516. That is, it goes low for the ninth-from-the-last horizontal line in a full screen display or the second horizontal panel in a split screen display. It marks the beginning of the bottom label field. This signal is output from A2A's pin 23. A complement of this signal is generated by driving inverting buffer X25Y54A with LSL/ to produce LSL.

A2A's Pin 18 Output : A2A's pin 18 output is a part of the OEF (Odd/Even Field) circuitry consisting of:

- A2A's pin 18
- OR gate X37Y9D
- counter X43Y38 (section D)

This logic functions as a toggle flip-flop that is clocked by the rising edge of the last pixel of each vertical frame. The result is a symmetrical square wave that changes state at the end of each vertical frame.

OEF is fed into A2A where it is combined with line count 524. A2A's pin 18 output goes low during line 524 of every other frame (during the frame that OEF is high). OR gate X37Y9D reduces the width of this gate to one pixel by ORing it with HCR/. HCRDLY/, the output of the OR gate, drives the preset input (pin 6) of the QD section of counter X43Y38. This counter stage functions as a D-type latch that is clocked by VCR. As an example of how this logic interacts, assume that OEF is currently high. During line 524, A2A’s pin 18 goes low. During pixel 779 of line 524, HCR/ goes low causing the output of OR gate X37Y9D to go low. At the end of pixel 779, VCR goes high, latching the low into counter X43Y38’s D section. OEF is now low (beginning of a new frame pair).

HCRDLY/ : See Timing Diagram 5 on the adjacent page. HCRDLY/ (Horizontal Count Reset Delay) is the output of OR gate X37Y9D. This signal is described in the A2A’s pin 18 output description above.
Timing Diagram 6. PAL A1 Timing
A2A’s Pin 14 Output

A2A’s pin 14 output is asserted when the count from X43Y25 (8 LSBs) and X43Y38 (2 MSBs) reaches 524. This output is combined with HCR to produce VCR. The two vertical counter chips (X43Y25 and X43Y38) are reset to zero during the last pixel of line 524 by VCR. This results in a vertical range of 0-524, a total of 525 lines. Thus, A2A’s pin 14 output defines the number of horizontal lines in a frame.

VCR

See Timing Diagram 5 on page 5-12. VCR (Vertical Count Reset) is the output of OR gate X45Y66D. The inputs to this gate are A2A’s pin 14 output and HCR. A2A’s pin 14 is low during the last line of the vertical frame. HCR goes low during the last pixel of each line. Therefore, VCR goes low during the last pixel of the last line of the vertical frame.

OEL

See Timing Diagram 5 on page 5-12. OEL (Odd/Even Line) is generated by the D-stage of counter X43Y73 and NAND gate X41Y18C. These components function as a toggle flip-flop. The NAND gate provides phase inversion and field synchronization. HCRDLY is low only during the last pixel of the last line of a two-frame pair. Regardless of the other input, the NAND gate generates a high output during the last pixel of a two-frame pair. This high output is latched into the counter on the trailing rising edge of HCR. Thus, the counter will always start a frame pair with OEL high (with a possible exception of the first frame pair following power up). Thereafter, OEL toggles at the end of each horizontal line.

Refresh Control

Refresh Control is accomplished by PAL A1 located at X45Y1. Refer to the PAL A1 equations in the Reference section of this manual and Timing Diagram 6 on the adjacent page. PAL A1 generates the following signals:

- WEXRF/(WIDE WORD External Refresh)
- WREN/(Write/Read Enable)
- RRST/(Raster Read Start)
- FI (Frame Interval)
- VI (Vertical Interval)

WEXRF/

The PAL equation for WEXRF/ is:

!WEXRF/ = HRG & ((Address=^h14) & (Address#37) & (Address#38) & (Address#3B))

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The first term causes WEXRF/ to go low if HRG is high and the pixel address is 20-55 (decimal); the second term causes WEXRF/ to go low if HRG is high and the pixel address is 56-59 (decimal). Combined, the two terms cause WEXRF/ to go low if HRG is high and the pixel address is 20-59 (decimal).

The equation for HRG (Horizontal Refresh Gate) is:

\[ !HRG = \text{Address} == ^h46 \]
\[ # !HRG \& \text{HCR} \]

The first term forces HRG low on pixel 70 (decimal); the second term holds HRG low until the end of the current line is reached. At that time, HCR goes low, releasing the hold. Thus, HRG is high from pixels 0-69 (decimal). HRG is necessary because the PAL does not have enough inputs to monitor all 10 Horizontal Counter inputs. By using the 7 LSBs and the internally generated HRG, WEXRF/ is limited to pixels 20-59 (decimal), a total of 40 pixel clock periods.

While WEXRF/ is low, the WIDE WORD memory performs refresh cycles. Dataram's refresh specifications require 600 nsec for each refresh cycle except the last which must be at least 100-200 nsec in duration. Thus, three refresh cycles require a 1500 nsec minimum. The 40 pixel clock periods allow 1629 nsec, insuring that three refresh cycles are generated during the horizontal blanking time of each scan line. The time between pixel periods 60 and 67 (about 325 nsec) provides time for completing the last refresh cycle. Dataram specifies a minimum of 256 refresh cycles every 4 msec. In that time, 125 horizontal scan lines are generated, enabling 375 refresh cycles.

**RRS/**

RRS/ goes low during pixel period 69 (decimal) of each scan line beginning with scan line 43. RRS/ initiates the first of three Sequential Read cycles generated by the Raster Read Sequence Control logic and asserts RRE/. The completion of the first cycle initiates the second; the completion of the second cycle initiates the third. Upon completion of the third cycle, RRE/ goes high.

**WREN/**

WREN/ informs the B Board that the A Board has finished its line read of all three channels. This signal is asserted when HRG is low (pixel periods 70-779) and RRE/ (Raster Read Enable) is high.

**FI**

FI goes low during lines 0-42 if OEF is low. OEF is low during the first frame of a frame pair. Thus, FI has a rate of about 30 Hz. FI is used by the B Board and as an interrupt for the PS/2.

**VI**

VI goes low during lines 0-42 of every frame. VI is used exclusively by the B Board. It has a rate of about 60 Hz.
Cursor Generators

Cursor Generators 0 and 1 are shown on schematic sheets 4 and 5, respectively. Also refer to Figure 9 on page 4-26 and the applicable PAL equations. Since the Cursor Generators are identical, only Cursor Generator 0 is described.

Horizontal Start Latch

The Horizontal Start Latch is a 10-bit D-type latch located at X37Y52. The latch is clocked by C0HP (Cursor 0 Horizontal Position). See Table 13 on page 5-2 for information on C0HP.

The latch's D-inputs are driven by the FIFOed Data bus (FD00-FD09) and contain the offset from the rising trailing edge of HCR/ to the left boundary of the cursor. The latch's outputs are connected to the preset inputs of the Horizontal Counter consisting of X37Y41, X33Y32 and X35Y56. The inputs to this counter are multiplexed, requiring that X37Y52 be a tri-state device. HCR/ drives the tri-state input of X37Y52 (pin 1). Thus, this latch drives the Horizontal Counter inputs only when HCR/ is low.

Moving the cursor involves changes in the offset (horizontal and/or vertical). As an example, consider moving a cursor from right to left across the screen. As the cursor moves, the horizontal offset decreases. At all times, it is equal to the cursor's center pixel position minus the cursor's horizontal half-width, e.g., a 300 pixel wide cursor centered at pixel 375 has a horizontal offset of 225. Since the first 128 pixels of the offset are always blanked by horizontal blanking, there are 97 visible pixels between the left edge of the screen and the left boundary of the cursor at this time. Note that the horizontal offset becomes zero when the cursor is centered at pixel 150. At this point, the cursor's center pixel is still 22 pixels away from the left edge of the screen. Any further movement to the left is accomplished by modifying the left half-width of the cursor. This is done by forcing the initial horizontal state to 3 and loading the modified half-width value into the Horizontal Start Latch. Setting the initial horizontal state to 3 inhibits the first download from the Horizontal Width Latch to the Horizontal Counter that normally occurs when the horizontal state is 4 and the horizontal offset has decremented to zero. Thus, the Horizontal Counter treats its initial loading from the Horizontal Start Latch by HCR/ as the first half-width. Moving the cursor any farther to the left causes the PS/2 to adjust this value from 150 towards 128 as the cursor's center pixel moves left to the edge of the screen. The PS/2 does not allow any further movement to the left once the cursor's center pixel is at the left edge of the screen.
Horizontal Width Latch

The Horizontal Width Latch is located at X35Y43. It is identical to the Horizontal Start Latch except for control signals and function. Its tri-state outputs are also multiplexed inputs to the Horizontal Counter. FD00 - FD07 (FIFOed Data bits 0 - 7) are latched into X35Y43 on the rising edge of C0HS (Cursor 0 Horizontal Size - see Table 13 on page 5-2. X35Y43's outputs are enabled by HCR. HCR is low (enabling X35Y43) at all times except during the last pixel period of each horizontal scan line.

Horizontal Counter

The Horizontal Counter consists of the three cascaded 4-bit synchronous up/down counters located at X37Y41, X33Y32 and X35Y56. These counters operate in the count down mode and are clocked by PXLCLK-N. Pin 23 of PAL A7, the State Decode PAL, enables the counters by driving pins 7 and 12 of X37Y41 low. Normally, the Horizontal Counter is loaded three times during each horizontal line. However, if the cursor is moved onto or past the left edge of the screen, the counter may be loaded only twice as described in the next paragraph. Prior to the start of a scan line, the Horizontal Start Latch provides a horizontal offset count from the rising trailing edge of HCR to the left edge of the cursor boundary. The counter counts this offset down at the pixel clock rate. Upon reaching zero, the counter is loaded with the output of the Horizontal Width Latch. Again, the counter counts down at the pixel clock rate. Upon reaching zero, the vertical center line of the cursor is reached. Finally, the counter is once more reloaded with the width data and allowed to count down at the pixel clock rate. This time, the right edge of the cursor is located when the counter reaches zero. Thus, the counter is loaded three times for each scan line, once for the offset and twice for the total width of the cursor.

Cursors having a total width exceeding 256 pixels can cause the Horizontal Counter to be loaded only twice if the cursor is slewed off the left edge of the display. Refer to the example described in the Horizontal Start Latch description.

The counter is configured as two cascaded sections. X37Y41 (least significant) and X33Y32 form the first section and function as an 8-bit counter; X35Y56 forms the second section and functions as the 2 MSBs of the Horizontal Counter. For counting purposes, the two sections are cascaded; for loading purposes, they are separate. This allows the 2 MSBs of the Horizontal Counter, upon decrementing to zero, to become the 2 LSBs of the Horizontal State Counter.
The Q-outputs of X37Y41 and X33Y32 are used only during a Cursor Construct readout. Standard cursor generation only requires an indication that the counter has decremented to zero. This condition is detected by OR gates X39Y54A and X39Y54B, and AND gate X39Y1A.

There are two load control signals for the Horizontal Counter, one for each of the sections described above. The output of AND gate X39Y1C drives the load pin (pin 11) on X37Y41 and X33Y32; HCR/ drives the load pin (pin 9) on X35Y56. When HCR/ goes low, all three counters have their load input enabled. At this time, the output of the Horizontal Latch is enabled, making the offset data available to the counter. The counter is loaded with offset data on the rising edge of the pixel clock pulse that occurs just prior to the end of HCR/.

Since HCR/ occurs only once each horizontal scan, X35Y56 is not reloaded when width data is loaded.

When decrementing, the RCO (Ripple Carry Output) of X33Y32 goes low each time the count in X37Y41 and X33Y32 reaches zero. This causes the pin 5 input of OR gate X39Y54B to go low. Via AND gate X39Y1A and OR gate X39Y54A, pin 4 of the OR gate goes low when counter X35Y56's QA and QB outputs (2 MSBs of the count) go low. Thus, a low at the output of OR gate X39Y54B indicates that the Horizontal Counter has reached zero. When the OR gate's output goes low, AND gate X39Y1C's output goes low, causing counters X37Y41 and X33Y32 to be loaded with width data (output of X35Y43).

**Horizontal State Counter**

The Horizontal State Counter consists of counter X35Y56. The QA (LSB), QB and QC (MSB) outputs of this chip, along with the RCO output of X33Y32 define the horizontal state codes shown in Table 4 on page 4-27.

When the horizontal offset is loaded into the Horizontal Counter, the C, B and A inputs of X35Y56 are preset to FJI, where F is the Edge Flag, and J and I are the MSB and second MSB of the horizontal offset, respectively. The Edge Flag defines the function of J and I. If the Edge Flag is high while X35Y56 is being loaded, J and I function as the two MSBs of the horizontal offset as described above; if the Edge Flag is low while X35Y56 is being loaded, J and I function as the MSB and LSB, respectively, of the Horizontal State count.

For horizontal offsets greater than 255, J or I (never both simultaneously) is high, resulting in a preset count of 5 or 6.

The QA (LSB), QB (second LSB) and QC (MSB) inputs from X35Y56 form a three-bit state count input to PAL A7, the State Decode PAL.
When the Horizontal Counter's offset decrements below 256 (decimal), OR gate X39Y54A's output goes low, driving the output of AND gate X39Y1A low. At this time, the horizontal state code is 4. When the offset count in X37Y41 and X33Y32 decrements to zero, X33Y32 drives its RCO output low (at the cursor's left boundary). On the next rising edge of PXLCK-N, X35Y56 decrements to 3 and X37Y41 and X33Y32 are preset with width data. Note that AND gate X39Y1A's output remains low because QC is low. This condition remains throughout the rest of the scan, isolating the Q outputs of X35Y56 from the Horizontal Counter's load strobe logic. That is, as long as PAL A7's pin 23 (counter enable) is low, X37Y41 and X33Y32 decrement on each PXLCK-N clock pulse and reload themselves with width data each time the RCO output of X33Y32 goes low. Each time RCO goes low, X35Y56 decrements. When X35Y56 decrements to 1, A7 disables X37Y41 and X33Y32, preventing further counting until the next scan.

In summary, the horizontal state normally begins in state 4 but may begin in state 3 when the cursor is moved off the left edge of the display. The horizontal state decrements to 1 while scanning the cursor. It decrements to 3 when the left edge of the cursor is reached; it decrements to 2 when the center line of the cursor is reached; it decrements to 1 when the right edge of the cursor is reached. Table 4 shows that by monitoring the outputs of X35Y56 and RCO, A7 can determine where the scan is relative to the cursor.

Edge Flag Latch

The Edge Flag Latch consists of both sections of a dual D-type latch located at X45Y106. The A-section forms the Horizontal Edge Flag; the B-section forms the Vertical Edge Flag. Each latch stores FD0A at the same time its respective offset latch stores FD00 - FD09. Note that the flags are inverted by using the complemented output from the latches.

Vertical Start Latch

The 10-bit latch located at X37Y28 is the Vertical Start Latch. It is identical to the Horizontal Latch. The Vertical Start Latch is loaded with vertical offset (from the top of the screen to the top of the cursor) from the FD bus when COVP (Cursor 0 Vertical Position) goes from low to high. This latch is enabled only during the time LSL/ (Label Start Line) is low. LSL/ is low during the ninth-from-the-last scan of the current frame.
Vertical Height Latch

The 10-bit latch located at X33Y43 is the Vertical Height Latch. It is identical in operation to the Horizontal Width Latch except it is loaded when COVS (Cursor 0 Vertical Size) goes high, and its output is enabled when LSL is low. LSL is low at all times except during the ninth-from-the-last scan.

Vertical Counter

The Vertical Counter consists of X37Y17, X35Y32 and X33Y56. The operation of this counter is similar to Horizontal Counter chips X37Y41, X33Y32 and X35Y56, respectively. The Vertical Counter decrements at the end of each HCR pulse.

The primary difference between the Vertical and Horizontal counters is that the AND and OR gates associated with the Horizontal Counter are replaced by PAL A8 (X33Y21). A8's pin 12 output corresponds to the output of AND gate X39Y1C in the Horizontal Counter logic. Using DeMorgan equivalents, the functions of the four gates are implemented by a NOR gate that is driven by:

- LSL/(X33Y21 pin 5)
- Vertical Ripple Carry Out (X33Y21 pin 1)
- X33Y56's QC output (X33Y21 pin 3)
- X33Y56's QB output (X33Y21 pin 7)
- X33Y56's QA output (X33Y21 pin 6)

As in the Horizontal Counter, X33Y56 functions as the two MSBs of the Vertical Counter as well as the Vertical State Counter. A7, the State Decode PAL, via its pin 14 output controls vertical counting by driving X37Y17's pins 7 and 12.

Vertical State Counter

The Vertical State Counter consists of X33Y56. Its operation is similar to the Horizontal State Counter. The state outputs are the QA, QB and QC outputs of X33Y56 (pins 14, 13 and 12, respectively). The Vertical State Outputs are interpreted by A7, the State Decode PAL.
State Decode PALs

The State Decode PALs consist of part of PAL A8 located at X33Y21 and PAL A7 located at X31Y7. PAL A8 latches the Cursor Type and passes it to PAL A7. The Cursor Type selects one of the five cursors shown in Figure 8 on page 4-24, or the Construct Cursor or its inverse. The Cursor Type is carried on the three LSBs of the FD bus and is latched into A8 when COT (Cursor 0 Type) goes low. Pins 14-16 of A8 are the latched results of FD00-FD02, respectively.

PAL A7 receives latched Cursor Type information from PAL A8, horizontal and vertical state inputs from the state counters, and the RCO (Ripple Carry Out) from each counter. It uses combinations of the inputs to define each of the following attributes:

- upper left pixel
- top line
- center pixel of the top line
- left side
- vertical center line
- right side
- left side center pixel
- horizontal center line
- center pixel
- bottom line
- solid box
- top center line (top of screen to top of cursor)
- bottom center line (bottom of cursor to bottom of screen)
- left center line (left edge of screen to left edge of cursor)
- right center line (right edge of screen to right edge of cursor)
As an example, the upper-left pixel (point A in Figure 19) is detected when:

- the horizontal RCO is low (horizontal offset decremented to zero), and
- the horizontal state code = 4, and
- the vertical RCO is low (vertical offset decremented to zero), and
- the vertical state code = 4.

One or more of the attributes define each of the standard cursors shown in Figure 8. Each of the standard cursors, the constructed cursor, the complement of the constructed cursor and Cursor Off are tri-stated outputs of PAL A7. These outputs are tied together and labeled CUR0. The latched 3-bit Cursor Type output from PAL A8 determines which tri-state output of PAL A7 is enabled. Table 5 on page 4-29 defines the Cursor Type.

**Construct RAM**

The Construct RAM is a 64K by 1 bit static RAM located at X33Y9. Addressing of the RAM is multiplexed. During programming, its address inputs are driven by line drivers located at X35Y21 (8 LSBs) and X35Y10 (8 MSBs); during readout, its address inputs are driven by the Horizontal and Vertical Counters, and PAL A8. PAL A8 drives the RAM's A7 (F7) and A15 (H7) inputs. It also provides two tri-state drivers for the RAM. These drivers are enabled by DVG/, the same signal that enables the outputs of the Horizontal and Vertical Counters. X33Y56's QA output (pin 14 - LSB of the Vertical state code) drives H7; X35Y56's QA output (pin 14 - LSB of the Horizontal state code) drives F7. Thus, the MSB of a respective counter's input is the LSB of it's state code. This scheme prevents readdressing the same section of the RAM each time the height and width values are reloaded.

The diagram on the next page shows the values of F7 and H7 in each quadrant of the cursor. Several address points, labeled A-I, are also shown.
Table 15 below defines the Construct RAM’s address for each point in the diagram above. The addresses shown are for a 256 by 256 pixel cursor. Regardless of cursor size, use the horizontal width as the A0-A6 address inputs and the vertical height as the A8-A14 address inputs. The A7 and A15 inputs are defined by the LSB of the Horizontal and Vertical state counts, respectively. The diagram above shows the quadrants, the LSBs of the horizontal and vertical state counts (F7 and H7 respectively) and the horizontal and vertical states.

<table>
<thead>
<tr>
<th>Point</th>
<th>Address (hex)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>FF 7F</td>
<td>First pixel of top line in quadrant 3</td>
</tr>
<tr>
<td>B</td>
<td>FF 80</td>
<td>Last pixel of top line in quadrant 3</td>
</tr>
<tr>
<td>C</td>
<td>FF 7F</td>
<td>First pixel of top line in quadrant 2</td>
</tr>
<tr>
<td>D</td>
<td>FF 00</td>
<td>Last pixel of top line in quadrant 2</td>
</tr>
<tr>
<td>E</td>
<td>FF 80</td>
<td>First pixel of last line in quadrant 3</td>
</tr>
<tr>
<td>F</td>
<td>FF 7F</td>
<td>Last pixel of last line in quadrant 3</td>
</tr>
<tr>
<td>G</td>
<td>FF 7F</td>
<td>First pixel of top line in quadrant 1</td>
</tr>
<tr>
<td>H</td>
<td>FF 00</td>
<td>Last pixel of last line in quadrant 1</td>
</tr>
<tr>
<td>I</td>
<td>FF 00</td>
<td>Last pixel of last line in quadrant 0</td>
</tr>
</tbody>
</table>

Table 15. Construct RAM Address Mapping
Label Generator

The Label Generator is shown on sheet 6 of the A Board schematics. Also refer to Figure 10, the Label Generator Functional Block Diagram, on page 4-30 as necessary.

Character RAM

The 8K byte static RAM located at X25Y3 is the Character RAM. It stores up to 64, 106-character labels. During label storage, FD bus data passes through the Data Buffer, located at X20Y32, to the RAM’s D-inputs. At the same time, the FA address bits FA00-FA0C drive the A0-A12 inputs of the RAM, respectively, via the Address Multiplexer. CLD (Character Load Drive) enables FD bus data to the RAM by enabling the Data Buffer when it goes low. CLD stores this data in the RAM on its rising trailing edge. The RAM’s output is enabled during the last 8 lines of a frame by LVB/ (Label Vertical Boundary). LVB/ is shown in Timing Diagram 8 on page 5-30 and described in the Divide-by-Eight Line Counter description.

FD00-FD05 define the character during storage. FD07 is the blink flag. If FD07 is high, the character is blinked; if it is low, the character is displayed continuously. Table 16 shows the characters and their codes. If a character is to be blinked, add 80H to the code.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>00 (sp)</td>
<td>10</td>
<td>20 @</td>
<td>30 P</td>
</tr>
<tr>
<td>01 !</td>
<td>11 1</td>
<td>21 A</td>
<td>31 Q</td>
</tr>
<tr>
<td>02 &quot;</td>
<td>12 2</td>
<td>22 B</td>
<td>32 R</td>
</tr>
<tr>
<td>03 #</td>
<td>13 3</td>
<td>23 C</td>
<td>33 S</td>
</tr>
<tr>
<td>04 $</td>
<td>14 4</td>
<td>24 D</td>
<td>34 T</td>
</tr>
<tr>
<td>05 %</td>
<td>15 5</td>
<td>25 E</td>
<td>35 U</td>
</tr>
<tr>
<td>06 &amp;</td>
<td>16 6</td>
<td>26 F</td>
<td>36 V</td>
</tr>
<tr>
<td>07 ’</td>
<td>17 7</td>
<td>27 G</td>
<td>37 W</td>
</tr>
<tr>
<td>08 (</td>
<td>18 8</td>
<td>28 H</td>
<td>38 X</td>
</tr>
<tr>
<td>09 )</td>
<td>19 9</td>
<td>29 I</td>
<td>39 Y</td>
</tr>
<tr>
<td>0A *</td>
<td>1A</td>
<td>2A J</td>
<td>3A Z</td>
</tr>
<tr>
<td>0B +</td>
<td>1B ;</td>
<td>2B K</td>
<td>3B [</td>
</tr>
<tr>
<td>0C ;</td>
<td>1C &lt;</td>
<td>2C L</td>
<td>3C \</td>
</tr>
<tr>
<td>0D -</td>
<td>1D =</td>
<td>2D M</td>
<td>3D ]</td>
</tr>
<tr>
<td>0E .</td>
<td>1E &gt;</td>
<td>2E N</td>
<td>3E ~</td>
</tr>
<tr>
<td>0F /</td>
<td>1F ?</td>
<td>2F O</td>
<td>3F ^</td>
</tr>
</tbody>
</table>

Table 16. Label Character Codes
Address Multiplexer and Latch

The multiplexer consists of four 4-bit data selectors located at X17Y27, X17Y18, X17Y9 and X14Y23. VG (Vertical Gate) drives the select input (pin 1) of each chip. When VG is low, the A inputs drive the RAM’s address inputs; when VG is high, the B inputs drive the RAM’s address inputs. Since VG is low during scan lines 00-42, the A-inputs (FA00-FA12) drive the RAM during this time.

The Address Multiplexer gates FA00-FA0C to the RAM during character loading. During label readout, the multiplexer gates the following to the RAM:

- outputs of the Character Counter (drives RAM inputs A0-A6)
- outputs of the Latch (drives RAM inputs A7-A11)
- DTB (drives RAM input A12)

The Character Counter functions as a 7-bit character address generator. Although it has a range of 0-127 (decimal), it only uses the first 106 addresses.

The Latch, consisting of the D-type latch located at X20Y43, functions as a 5-bit label selector. FD bus data is latched when CLL (Character Label Load) goes high. The Latch’s outputs select one of 32, 128-byte label blocks. After a block (label) is selected, the Character Counter sequentially addresses the 106 characters in the block.

DTB selects a second bank of labels during split panel operation. DTB is low during a full screen display and the upper panel of a split screen display; DTB is high during the bottom panel of a split screen display. Thus, up to 32 frames can have up to two labels each.

 Divide-By-Six Pixel Counter

The Divide-By-Six Pixel Counter consists of a 4-bit binary synchronous up/down counter located at X17Y44 and AND gate X14Y7A. The counter operates in the down mode and decrements on the rising edge of PXLCK-A when its load input (pin 9) is driven high by the AND gate’s output. When the AND gate’s output goes low, the counter is preset to five.

AND gate X14Y44’s pin 1 is high during the last eight lines of the panel or full screen because the Line Counter’s (X20Y23) QD output (LVB/) is low during this time only (inverted by X25Y54E). For information on LVB/, see the Divide-By-Eight Line Counter description.
AND gate X14Y7A's pin 2 input is high except when X17Y44 underflows. Therefore, during the last eight scan lines of a panel or full screen, the AND gate's output is high except when X17Y44 underflows. This causes X17Y44 to repeatedly decrement to zero and reload itself at the pixel clock rate. That is, it reloads itself on every sixth pixel while label lines are being scanned. This includes the horizontal blanking period as well as the visible pixel portion. Since a horizontal line is defined as 780 pixels, the circuit divides each of the eight scan lines into 130, 6-pixel periods. Timing Diagram 7 on the next page shows the Divide-By-Six timing.

Character Counter

The Character Counter consists of a dual 4-bit cascaded up counter located at X17Y36 (sections A and B). Section A is clocked on the falling edge of X17Y44's QC output. Timing Diagram 7 shows that this signal goes high at the beginning of each character field. The counter is prevented from counting during the horizontal blanking time by applying LG/ to the counters' clear inputs (pins 2 and 12).

The horizontal blanking period is 140 pixels long (780-640=140). It begins with pixel 768 of the previous line and ends at the start of pixel 128 of the current line. X17Y44 begins counting at the beginning of the blanking period in which LVB/ goes low. During the first 138 blanked pixels, the Divide-By-Six Counter completes 23 complete cycles. These cycles are not counted by the Character Counter because LG/ is continuously clearing it at this time. During the last two blanked pixels (139-140), the Divide-By-Six Counter reloads a count of 5 and decrements twice, resulting in a count of 3 at the falling edge of LG/. Therefore, X17Y44's QC output goes high on the fourth visible pixel and every sixth pixel thereafter. Because the Divide-By-Six Counter is in the middle of the first character when LG/ goes low, the first character of each label should be a space (sp).
Timing Diagram 7. Divide-By-Six Counter Timing
Character PROM

The Character PROM, a 512 by 8-bit PROM, is located at X20Y12. The D0-D5 output of the Character RAM drives the six MSB address inputs of the PROM. Since the character's code drives these address inputs, each code selects an 8-byte block of the PROM. Once a block is selected, the output of the Divide-By-Eight Line Counter determines which byte is output to the Output Shift Register. As an example, consider the character "R." The Character RAM outputs a code of 32H for the character R, selecting addresses 190H-197H. The contents of each address is shown in Table 17 below.

<table>
<thead>
<tr>
<th>Address (hex)</th>
<th>Data (hex)</th>
<th>Line</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>190</td>
<td>1E</td>
<td>0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>191</td>
<td>11</td>
<td>1</td>
<td>*</td>
<td></td>
<td></td>
<td></td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>192</td>
<td>11</td>
<td>2</td>
<td>*</td>
<td></td>
<td></td>
<td>*</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>193</td>
<td>1E</td>
<td>3</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>194</td>
<td>14</td>
<td>4</td>
<td>*</td>
<td></td>
<td></td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>195</td>
<td>12</td>
<td>5</td>
<td>*</td>
<td></td>
<td></td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>196</td>
<td>11</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td>*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>197</td>
<td>00</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>*</td>
<td></td>
</tr>
</tbody>
</table>

* = high, (space) = low

Table 17. Character Formation Example
Timing Diagram 8. Label Field Generation
Divide-By-Eight Line Counter

The Divide-By-Eight Line Counter consists of the synchronous 4-bit binary up/down counter located at X20Y23 and AND gate X14Y7C. The counter operates in the up mode, and loads or counts on the rising edge of LG, the clock input.

LSI (Label Start Line) and LSS (Label Split Start) drive the output of the AND gate low during the eighth scan line from the bottom of the screen or panel, respectively. The rising trailing edge of LG (see Timing Diagram 7), occurs at the start of pixel 768. This edge clocks the counter, presetting it to zero. This asserts LVB, the counter's QD output. At the end of the current scan line, the AND gate's output returns high, placing the counter in the count mode. The counter increments near the end (pixel 768) of each scan line until it reaches 8. Then LVB goes high, disabling counting by driving pins 7 and 10 high. The Divide-By-Eight line Counter timing is shown in Timing Diagram 8 on the adjacent page.

Output Shift Register

The Output Shift Register is located at X20Y1. This chip has several modes of operation that are determined by its S0 and S1 (pins 1 and 19, respectively) inputs. Since S0 is tied high via PL2, only these two modes are used:

- shift right (S1 is low)
- load (S1 is high)

SR and SL are the serial data inputs for the shift right and shift left modes, respectively. The 6-bit parallel data output of X20Y12 drives the 6 MSB inputs of the shift register. If S1 goes high, this data is loaded into the shift register. Then, after S1 goes low, the data shifts right on the rising edge of PXLCK-A, shifting the data toward the MSB end. The MSB output is on pin 17 (QH). After six clock pulses, the bit initially loaded into pin 6 (C input) appears at pin 17. As the word shifts right, zeros stuff the LSBs because pin 11 is grounded. Therefore, after six shift pulses, zeros appear at the pin 17 output if the shift register isn't reloaded. This is what happens when blinking characters.
Blink Control

Blink Control is accomplished by AND gate X14Y7B and NOR gate X14Y15A. When a character is written to the Character Generator, its bit 7 status is used as a blink flag. During character readout, the blink flag drives pin 4 of the AND gate. Pin 5 of the AND gate is driven by the symmetrical square wave output (BINK) of the Blink Generator. The AND gate's output is low during nonblanked characters and during blinked characters when BINK is in the low half of its waveform.

Pin 3 of the NOR gate is normally high during label field scanning except during Divide-By-Six Pixel Counter reloading. Thus, during nonblanked conditions, the NOR gate's output is low except during Divide-By-Six Pixel Counter reloading. This causes a new character to be loaded into the shift register every six clock pulses. When the AND gate's output goes high, the NOR gate's output goes low regardless of its pin 3 input, keeping the shift register in the shift mode. Since the shift register isn't reloaded, zeros are shifted out until the shift register can be reloaded again.
Blink Generator

The Blink Generator is located on sheet 19 of the A Board schematics. It consists of a D-type octal latch located at X41Y90, an 8-bit binary counter located at X39Y77 and a D-type latch located at X39Y46B.

Latch X41Y90 is loaded with the blink rate on the rising edge of BRL (Blink Rate Load - see Table 13 on page 5-2). The latch's outputs drive the preset inputs of the counter.

The counter operates in the count down mode. Since TC (Terminal Count - pin 14) is connected to PE (Parallel Enable), the counter presets itself to the latch's output value each time it decrements to zero. VCR (Vertical Count Reset) clocks the counter at a rate of 59.94 Hz. Therefore, TC goes low at a rate of 1/59.94 to 4.27 seconds for latch values of 0-255, respectively.

The D-type latch is wired as a toggle flip-flop by connecting its Q output to its D input. This D-type latch divides the output frequency of the counter's TC output by two and converts the counter's asymmetrical output to symmetrical output. Based on the output rates described above, the D-type latch has an output rate of 1/29.97 to 8.54 seconds.
Raster Read Section

Refer to sheets 7 through 12 of the A Board schematic diagrams, Figure 6 on pages 4-13 and 4-14, Figure 13 on page 4-42 and Figure 15 on page 4-46 as necessary.

Raster Read Start Address Files

The Raster Read Start Address Files, shown on sheet 7 of the schematics, consist of 8 cascaded 4-bit by 16-word static RAMs. They function as a 16-word by 32-bit RAM. The FD bus inputs the start addresses to the files. Since start addresses are 32 bits wide and the FD bus is only 16 bits wide, a double write cycle is required to write one start address. The lower 16 bits are stored when LSA (Lower Start Address) goes low; the upper 16 bits are stored when USA (Upper Start Address) goes low. The chips strobed by LSA are:

- X8Y33 (bits 0-3)
- X10Y17 (bits 4-7)
- X8Y25 (bits 8-B)
- X10Y9 (bits C-F)

The chips strobed by USA that store the upper 16 bits are:

- X8Y17 (bits 10-13)
- X10Y1 (bits 14-17)
- X8Y9 (bits 18-1B)
- X8Y1 (bits 1C-1F)

All 16 chips are enabled simultaneously when SAG/ (Start Address Gate) goes low. SAG/ is described in the Raster Read Line Address Generator description below.

The files are addressed by LA0-LA2 (Load Address bus), the outputs of the File Address Multiplexer. This 3-bit addressing bus provides an 8-word addressing capability. Because the A3 input of each chip is grounded, only the first six words are used. The files provide storage for two start addresses for each of the three channels, a start address for the upper panel or full screen and a start address for the lower panel. Table 7 on page 4-41 shows the address to channel mapping. For additional addressing information, refer to the File Address Multiplexer description below.
Raster Read Line Length and Zoom Factor Files

The Raster Read Line Length and Zoom Factor Files are shown on sheet 8 of the A Board schematics. The Raster Read Line Length Files consist of four cascaded 4-bit by 16-word static RAMs. Together, these RAMs function as a 16-word by 16-bit RAM. The chips that comprise the Raster Read Line Length Files are:

- X10Y41 (bits 0-3)
- X12Y15 (bits 4-7)
- X10Y33 (bits 8-B)
- X12Y7 (bits C-F)

Raster Read Line Length File addressing is identical to the Raster Read Address Files addressing scheme described on the previous page.

The FD bus provides line length data to the D inputs. This data is stored on the rising edge of LLL (Line Length Load). The line length files are read when ZLG/ (Zoom Load Gate) goes low. The 16-bit line length provides a line length range of 00-64K WIDE WORDs (0 - 1,048,576 pixels).

The Zoom Factor File consists of a 4-bit by 16-word static RAM located at X10Y25. FD00-FD03 are loaded into the RAM on the rising edge of ZFL (Zoom Factor Load). Addressing of this RAM is identical to the addressing of the Raster Read Start Address and the Raster Read Line Length Files. Note that the tri-state enable for the Zoom Factor File is grounded. Thus, the ZF (Zoom Factor) bus is not tri-stated. This is not possible with the start address and line length files because their outputs are multiplexed (see the Raster Read Address Generator description on page 5-37).

File Address Multiplexer

The File Address Multiplexer consists of a read address generator located on sheet 8 and a 4-bit multiplexer located on sheet 7 of the A Board schematics.

The read address generator generates LS0 and LS1, a 2-bit address code that identifies the channel currently being processed by the Raster Read section. LS1 (MSB) and LS0 (LSB) are inputs to the multiplexer on sheet 7.
The read address generator consists of a dual D-type latch located at X17Y1. These latches are wired as a 2-bit down counter. The negative HCR/ (Horizontal Count Reset) pulse resets both sections of X17Y1, making LS1 high and LS0 low. This is the initial address at the beginning of each horizontal scan. RLFL (Raster Line FIFO Load) goes from low to high at the end of each channel's fetch cycle. This transition clocks both latches. Since three channels are fetched each horizontal line, the latches are clocked twice during each horizontal scan. Table 18 shows the count after each clock pulse.

<table>
<thead>
<tr>
<th>Clock</th>
<th>LS1, LS0</th>
<th>Channel*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial</td>
<td>1 0</td>
<td>2, C, Image 2</td>
</tr>
<tr>
<td>First</td>
<td>0 1</td>
<td>1, B, Image 1</td>
</tr>
<tr>
<td>Second</td>
<td>0 0</td>
<td>0, A, Graphics</td>
</tr>
</tbody>
</table>

* Channels switch designators as the signals progress toward the output connectors.

Table 18. Channel Address to Channel Designator Map

The multiplexer multiplexes the read and write addresses to the Raster Read Start, Raster Read Line Length and Raster Read Zoom Factor Files. Multiplexer switching is accomplished by VG/which is low during the visible scan lines and high during the vertical blanking time. During the vertical blanking time, the multiplexer's B-inputs drive the LA bus. During this time, FA08-FA0A drive the address inputs of the files. During the visible scan line time, LS1 and LS0 drive the A2 and A1 inputs of the files, respectively. Thus, two file addresses are assigned to each LS address (channel address).

DTB (Delayed Top/Bottom) drives the A0 input of the files. DTB is low during full screen display modes and during the upper panel of split screen modes. When DTB is low, the start address, line length and zoom factor for the upper panel or full screen are addressed; when DTB is high, the start address, line length and zoom factor for the lower panel are addressed.
Raster Read Address Generator

The Raster Read Address Generator is located on sheet 9 of the schematics. Also refer to Figure 6 (pages 4-13 and 4-14) and Figure 13 (page 4-42) as necessary.

The 4 LSBs of the memory address (MA00-MA03) are used as a byte address during disassembly of WIDE WORDs. That is, they are not part of the address sent to the WIDE WORD memory. MA04-MA1F address the WIDE WORD memory. This 28-bit Sequential Read start address is driven by the output of the Raster Read Address Generator. The generator generates the start address for each of the three channels by adding a channel's line length or zero to its previous address. A new address is output to the memory at the beginning of a channel's Sequential Read cycle. It is also stored for use during the next line's address generation.

Components

The generator contains seven cascaded 4-bit adders located at X4Y48 (4 LSBs), X4Y39, X4Y30, X6Y9, X4Y21, X4Y12 and X4Y3 (4 MSBs). The chips are cascaded by wiring the bit 4 carry output (pin 9) of a chip to the bit 0 carry input (pin 7) of the next higher ordered chip.

The sum output of each adder chip drives the D-inputs of a 4-bit by 16-word FIFO. These FIFOs make up the Next Line Start Address FIFO (see Figure 13 on page 4-42). The cascaded FIFOs function as a 28-bit by 16-word FIFO. In an increasing order of significance, the FIFOs are located at X2Y48, X2Y39, X2Y30, X6Y1, X2Y21 and X2Y12. The FIFOs drive the WIDE WORD memory's address bus via the WIDE WORD Memory Address Bus Drivers located on sheet 12 of the schematics. Each FIFO also drives the B-inputs of its respective adder chip. Collectively, the 28 FIFO output bits drive the 28 B-inputs of the adder.

The adder's 16 LSB A-inputs are driven by the LL (Line Length) bus which has multiplexed inputs. It is driven by the Raster Read Line Length Files or the outputs of line drivers X6Y18 and X6Y29. These line drivers drive the LL bus with zeros during line replication. Thus, the adder's output equals the previous start address plus line length, or the previous start address plus zero.

The Zoom Factor State Machine, consisting of a 512-byte PROM located at X6Y40, and a 4-bit by 16-word FIFO located at X8Y42, determines whether the Raster Read Line Length Files or zeros drive the LL bus.
The MA bus is multiplexed. It is driven by the outputs of the Next Line Start Address FIFO or the Raster Read Start Address Files. The tri-state outputs of the FIFOs are enabled when AND gate X14Y7D goes high. DVG, the pin 12 input to the gate, is high during scan lines 44-524 (visible scan lines). HSI/ is high at all times except during the last line of the upper panel in a split screen display. Therefore, the Raster Read Start Address Files drive the MA bus and the adder's A-inputs during vertical blanking and during the last scan line of the upper panel in a split screen display. At all other times, the Next Line Start Address FIFO's output is enabled. SAG/ (Start Address Gate), which is AND gate X14Y7D's output, enables the output of the Raster Read Start Address Files (see sheet 7 of the schematics) at the same time it tri-states the output of the Next Line Start Address FIFOs.

During the last blanked vertical line (line 43), the File Address Multiplexer (see sheet 7) switches to the A addressing source, addressing Channel C. At this time, SAG/ is low, presenting Channel C's start address to the Raster Read Address Generator via MA04-MA1F. At this time, the LL bus is driven by either the output of the Raster Read Line Length Files (zoom factor of zero only) or the output of the zero line length drivers (nonzero zoom factors).

This causes the adder's output to equal its B-input address (nonzero zoom factors) or its B-input address plus line length (zero zoom factor). This address is presented to the FIFO while the start address on the MA bus is presented to the input of the WIDE WORD Memory Address Bus Drivers. The adder's output, Channel C's next line start address, is not available to the MA bus at this time because the FIFO's output is tri-stated. RLFL (Raster Line FIFO Load) goes high at the end of the Channel C fetch cycle, clocking Channel C's new start address into the FIFO.

The rising edge of RLFL clocks the file read address generator, decrementing its count from 10 (binary) to 01 (binary). This address addresses Channel B's start address file. The Channel B cycle is identical to the Channel C cycle, resulting in the Channel B's start address driving the Dataram memory and its next line start address being stored in the Next Line Start Address FIFO. Upon completion of the Channel B cycle, the process is repeated for Channel A. At the completion of line 43 (last vertical blanking line), the Next Line Start Address FIFO contains the start address of the next line of all three channels.
At the start of line 44 (first visible line), SAG/ goes high, enabling the Next Line Start Address FIFO and disabling the output of the Raster Read Start Address Files. As soon as the FIFO is enabled, it drives the MA bus with Channel C's next address (start address plus line length or zero). The adder sums this address with the line length (zero or the frame's actual line length) and presents it to the FIFO.

RLFD (Raster Line FIFO Done) and RLFL are identical except that RLFD, the FIFO unload clock, is inhibited during line 43. Therefore, during the visible lines (lines 44-524), the next address for the current channel is stored at the same time the next line address for the next channel is unloaded. Thus, Channel C's third visible line start address is stored at the same time Channel B's second visible line start address is unloaded. The process is repeated for Channel A. This entire process is repeated through visible line 480 (raster line 524) for full screen displays or until the end of the upper panel is reached. For split screen displays, HSI/ goes low during the last line of the upper panel, downloading the lower panel's start address. Then, the address generation process continues, as described above, until visible line 480 is completed.

Line length multiplexing (zero or the frame's line length) is controlled by ZLG (Zero Line Gate). When ZLG is low, the zero line drivers (X6Y18 and X6Y29) drive the LL bus; when ZLG is high, the Raster Read Line Length Files drive the LL bus.

ZLG is the output of the Zoom Factor State Machine. OR gate X51Y55D forms ZLG by ORing the Q4 output of PROM X6Y40 with VG/. VG/ causes ZLG to be high during scan lines 00-42. From scan line 43 to 524, ZLG is a function of the PROM's Q4 output.

The Zoom Factor State Machine consists of PROM X6Y40 and a 4-bit by 16-word FIFO located at X8Y42. The FIFO provides storage for all three channels. Its output is the current channel's previous state. The previous state is used as an input by the PROM to determine the next state for the current channel. The next state output of the PROM is stored in the FIFO at the end of the current channel's Sequential Read cycle. Since the load, unload and reset inputs to this FIFO are the same as those of the Next Line Start Address FIFO, the Zoom Factor State Machine switches channels at the same time as the rest of the Raster Read Address Generator section.
The channel’s input zoom factor selects one of two possible 16-byte blocks of PROM. SAG/ determines which of these blocks is selected. When SAG/ is low (Raster Read Start Address), the 4-bit output equals the input zoom factor minus one for input zoom factors greater than zero. When SAG/ is low and the input zoom factor is zero, the PROM outputs $10_{16}$ (Q4 goes high), driving ZLG high. The FIFO stores the 4 LSB outputs of the PROM at the end of the channel’s Sequential Read cycle.

After SAG/ returns high, the other 16-byte block of PROM selected by the input zoom factor is used. For the first line of each channel after SAG/ goes high, the FIFO outputs the code stored for that channel when SAG/ was low. This code drives the 4 LSB address inputs of the PROM, causing the PROM to output a value that is one less than its 4 LSB input value. Therefore, the PROM and FIFO function as a down counter, decrementing each time the channel’s Sequential Read cycle completes.

Eventually, the PROM outputs a zero to the FIFO which is stored as described above. The next time this channel’s code is unloaded, the 4 LSB inputs to the PROM will be zero. This causes the PROM to drive its Q4 output high, enabling the Raster Read Line Length Files. The value sent to the FIFO at this time equals the input zoom factor, causing the count down cycle to start over at the input zoom factor. In summary, the LL bus is driven by the zero line drivers at all times except when the input zoom factor is reloaded into the FIFO.
WIDE WORD Address Bus Drivers

The WIDE WORD Address Bus Drivers are shown on sheet 12 of the schematics. This section consists of a PAL, three 10-bit inverting line drivers and an octal inverting line driver. The 10-bit line drivers are located at X4Y70, X4Y57 and X2Y57. The octal line driver and the PAL are located at X2Y72 and X12Y53, respectively. The line drivers are enabled by RRE/ (Raster Read Enable). In addition, X2Y57 must also be enabled by ARE (Address Real Enable). RRE/ is low during the three consecutive Sequential Read cycles; ARE is active low for existent memory addresses. The PAL remaps nonexistent memory addresses to existent memory addresses.

Workstations require memory boards in groups of four that may be populated with 256K or 1M DRAMs. Thus, available memory can range from 2 to 32 megawords. Full addressing range capability exists, regardless of the actual available memory. Thus, it is possible to address nonexistent memory when less than maximum memory is available. If this happens, the Dataram memory "hangs-up", requiring a reset to recover.

WAD00/-WAD31/ are the active low WIDE WORD Address lines that address the Dataram memory. WAD00/-WAD24/ can address the maximum memory of a WIDE WORD chassis. Dataram uses WAD25/-WAD31/ to daisy chain multiple memory units together. Since workstations use a single chassis, these lines are always high (off). MA04-MA17 drive WAD00/-WAD19/ via line drivers X4Y70 and X4Y57. These lines have a 1 megaword addressing range. Therefore, if at least one memory array board set is installed, MA04-MA17 cannot address a nonexistent memory address if none of the upper 12 address bits are asserted.

The upper 4 address bits (WAD28/-WAD31/) are never asserted since their inputs are grounded. Thus, a nonexistent memory address is possible only when one or more of X2Y57's MA inputs (MA18-MA1F) are asserted. If PAL X12Y53 detects a nonexistent address, it disables X2Y57's tri-state output. This causes X2Y57's outputs to float high (off). Under this condition, the memory address written to or read from is determined by X4Y70 and X4Y57. This remaps nonexistent memory addresses to existent memory addresses in the 0 to 1 megaword range.

The PAL enables X2Y57 if one or more address inputs (MA19-MA1B) are asserted and the address is valid. Under normal conditions, writing to nonexistent memory is prevented by the McIDAS-OS2 SETUP software. Thus, this logic normally acts as a backup.
The WSZ00/-WSZ10/ lines are the binary representation of the total number of 128K word blocks of memory available. The PAL uses WSZ04/-WSZ10/ and MA19-MA1F to determine the validity of the current address. WWWs can have up to 32 megawords of memory. This equates to 256, 128K word blocks and requires memory size lines WSZ00/-WSZ07/ to represent the maximum available memory. The remaining lines (WSZ08/-WSZ10/) are used only when multiple units are daisy chained together. Though WSZ04/-WSZ10/ connect to the PAL, only WSZ04/-WSZ07/ are used. Table 19 defines memory size in terms of WSZ04/-WSZ07/ and standard frames.

<table>
<thead>
<tr>
<th>07/ 06/</th>
<th>WSZ- 05/</th>
<th>04/</th>
<th>Memory (megawords)</th>
<th>Frames</th>
<th>Board Sets</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2MW</td>
<td>1*</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>4MW</td>
<td>2*</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>6MW</td>
<td>3*</td>
</tr>
<tr>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>8MW</td>
<td>4*,1**</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>10MW</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>12MW</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>14MW</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>16MW</td>
<td>800</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>20MW</td>
<td>2**</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>22MW</td>
<td></td>
</tr>
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<td>0</td>
<td>0</td>
<td>24MW</td>
<td>1200</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>26MW</td>
<td>3**</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>28MW</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>30MW</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>32MW</td>
<td>1600</td>
</tr>
</tbody>
</table>

* Board sets use 256K DRAMs.
** Board sets use 1M DRAMs.

Table 19. Memory Size Summary
For an address to be valid, its memory read/write address must be equal to or less than the maximum address for the board sets installed. PAL X12Y53 determines the number and type (256K or 1M DRAMs) of board sets installed by the WSZ04/-WSZ07/ code as shown in Table 19. Refer to the WWA13 PAL module in the Reference section of this manual. Functionally, PAL A13 contains a NOR gate that is driven by 6 AND gates. Each AND gate performs a validity check for a specific board set. No test is performed for the 100 frames entry in Table 19 because a failure of this test would imply no memory. Thus, AND gates test address validity at the 4, 6, 8, 16, 24 and 32 megaword limits. The AND gates' inputs are selected such that an AND gate's test passes when its output is low. All AND gates must have a low output to force the NOR gate's output high and enable X2Y57.

Line driver X2Y72 drives three mode and three handshake lines in addition to the two MSBs of the WIDE WORD address. The mode control lines are:

- WENSQ/ (WIDE WORD Enable Sequential)
- WASCD/ (WIDE WORD Ascending Sequential Synchronize)
- WREAD/ (WIDE WORD Read)

The handshake lines are:

- WADAV/ (WIDE WORD Address Available)
- WDTRQ/ (WIDE WORD Data Request)
- WDTAC/ (WIDE WORD Data Acknowledge)

Section 8 of X2Y57 functions as a line receiver for WDTAC/. WDTAC/ is an incoming handshake signal; see sheet 10 of the schematics.
Timing Diagram 9. Raster Read Sequence Control Timing
Raster Read Sequence Control

The Raster Read Sequence Control section is shown on sheet 10 of the
schematics. Throughout this description, refer to the schematics and
Figures 6 (page 4-13 and 4-14) and 15 (page 4-46).

Number of WIDE WORDs Lookup

The Number of WIDE WORDs Lookup consists of a 512-byte PROM
located at X41Y34. MA00-MA03, the pixel start address offset
portion of the Memory Address bus, drive the 4 LSB address inputs of
the PROM; ZF0-ZF3, the current channel’s zoom factor, drive A4-A7,
respectively. Thus, the PROM contains a storage location for each
possible combination of zoom factor and pixel start address offset.
Programmed into each storage location is the binary value of the
number of WIDE WORDs that must be read to form a scan line based
on the current start address offset and zoom factor. This number can
range from 3 to 41 (decimal) WIDE WORDs. It presets the Number
of WIDE WORDs Counter located at X41Y45.

Number of WIDE WORDs Counter

The Number of WIDE WORDs Counter consists of the synchronous
up/down counter located at X41Y45. The ground on pin 1 places the
counter in the countdown mode. Timing Diagram 9 on the adjacent
page shows the timing relationships of the clock, CET and CEP inputs.

The counter decrements on the rising edge of PXLCK-M if CEP and
CET are simultaneously low. CEP, driven by the RCO output of the
Sequence Cycle Length Counter (X43Y1), goes low at the end of each
phase of each Sequential Read cycle. CET is driven by the counter’s
own QG output. Because the G and H inputs are grounded, QG and
QH go low when the counter is preset and remains low until the
counter underflows (decrements through zero to 11111111b). Thus,
once the counter decrements through zero, the QG output inhibits
further counting until a new load pulse arrives.

The Number of WIDE WORDs Counter is preset to the number of
WIDE WORDs required for a scan line when AND gate X41Y1A’s
output goes low. Therefore, the counter is preset if either of the AND
gate’s inputs goes low. The AND gate’s pin 1 input goes low while
RRS/ is asserted (during pixel 69 of scan lines 43-524). This presets
the counter with the number of Image 2 WIDE WORDs. The AND
gate’s pin 2 input goes low each time the Y3 output of the 2- to 4-line
decoder located at X39Y9A goes low. This output goes low when its A
and B inputs are high and its G input is low. The B input goes high
after the Number of WIDE WORDs Counter decrements through zero.
The A input, driven by the RCO output of the Channel Counter
(X41Y9), is high until the beginning of the Graphics Channel’s
Sequential Read cycle.
X41Y45 decrements after each Image 2 WIDE WORD is fetched. Upon reaching zero, the last word for Image 2 is fetched. At the end of this fetch cycle, the counter decrements from zero to 11111111B, causing the B input of X39Y9A to go high. Upon completion of the Sequential Halt cycle for Image 2, the Sequence Cycle Length Counter's RCO goes low, causing X39Y9A's Y3 output to go low. This presets X41Y45 to the Image 1 WIDE WORD count. The counter decrements as described for Image 2. Upon decrementing through zero, it is preset to the Graphics WIDE WORD count. Again, the counter decrements to zero. This time, however, it is not preset because the RCO output of X41Y9 is low, inhibiting counting until the next RRS/.

Sequence Cycle Length Counter

The Sequence Cycle Length Counter consists of the synchronous 4-bit binary counter chip located at X43Y1. The ground on pin 1 programs the counter as a down counter. The counter, clocked by PXLCK-M, measures each phase of each Sequential Read cycle in terms of clock periods. The levels on the A, B, C and D inputs, when the load pin (pin 9) is low and the counter is clocked, determine the cycle period.

Timing Diagram 9 shows the Sequence Cycle Length Counter timing. Table 20 below shows the A, B, C and D inputs at the trailing edge of the load strobe for each Sequential Read phase.

<table>
<thead>
<tr>
<th>D</th>
<th>C</th>
<th>B</th>
<th>A</th>
<th>Decimal Value*</th>
<th>Cycle Time</th>
<th>Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>11</td>
<td>480 nsec</td>
<td>Sync</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>120 nsec</td>
<td>Read</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>11</td>
<td>480 nsec</td>
<td>Halt</td>
</tr>
</tbody>
</table>

*Since counter presetting is synchronous, the counter decrements to zero and presets on the next clock pulse. This results in one clock pulse in addition to the preset value.

Table 20. Sequence Cycle Lengths
Channel Counter

The Channel Counter consists of the synchronous up/down binary counter located at X41Y9. RRS/presets the counter to 2. The counter decrements on the rising edge of PXLCK-M that occurs during the trailing edge of Y3; see Timing Diagram 9 on page 5-44.

The RCO output of X41Y9 provides a Channel 0 indication to the 2- to 4-line decoder, a component of the Sequence Control Logic. This causes the Sequence Control Logic to terminate the Raster Read process at the end of the Graphics Channel's Sequential Read cycle.

In addition to the RCO output, the Channel Counter provides a 2-bit binary channel count input to a 2- to 4-line decoder located at X39Y9B. This decoder is enabled during the entire Raster Read process. Y2, Y1 and Y0 are low during Image 2, Image 1 and Graphics Channel Sequential Read cycles, respectively. These Y-outputs are inputs to the Zoom Factor Load Decoder and the Read FIFO Load Decoder (described below).

Read Control Interface

The Read Control Interface consists of the WIDE WORD Handshake Control and the Sequence Control blocks in Figure 15 on page 4-46. Because these sections interact, they are discussed together in the following description.

These sections primarily consist of inverting line driver X33Y1A, line drivers X39Y18F and X39Y18G, and D-type latches X35Y1A, X35Y1B and X39Y46A. In addition, they receive inputs from NAND gates X41Y18A, X35Y106C and 2- to 4-line decoder X39Y9A, components of the Sequence Control Logic. The NAND gates form a set/reset flip-flop that is set by RRS/ and reset by the Y2 output of X39Y9A. The latches and line drivers form the WIDE WORD Handshake Control.

Timing Diagram 10 on the next page describes the Sequential Control and Handshake timing for Channel C (Image 2) when the zoom factor is 15. Smaller zoom factors cause longer read cycles.
Timing Diagram 10. Sequential Read Timing
Double Strobe Generator

The Double Strobe Generator consists of D-type latches X39Y29A and X39Y29B, delay line X37Y1 and AND gate X41Y1D. Timing Diagram 10 shows the timing for this section.

Because WIDE WORD data is stored in the respective Channel FIFOs as two 64-bit words, two WIDE WORD Data Latch output enable strobes must be generated. One strobe enables the lower 64 bits to the Channel FIFOs; the other strobe enables the upper 64 bits to the Channel FIFOs.

WIDE WORD data is valid on the input of the WIDE WORD Data Latches when WDTAC/ goes low. This data is latched into the WIDE WORD Data Latches on the trailing edge of WDTAC/. WDTAC/ is also buffered by line receiver X39Y18F and inverted by X25Y54F to form WWL (WIDE WORD Latch). The leading rising edge of WWL triggers the Double Strobe Generator.

The static condition of the D-type latch X39Y29A is determined as follows. If a low is assumed at the pin 6 (Q/) output, that low propagates through delay line X37Y1, causing pin 10 of the delay line to go low 30 nsec later. The low at pin 10 of the delay line resets X39Y29A, making its pin 6 output go high. The high at pin 6 propagates through the delay line, causing the D- and clear-inputs to go high. This is the static condition of X39Y29A.

Refer to Timing Diagram 10. The rising edge of WWL clocks X39Y29A, driving its pin 6 low. Thirty nanoseconds later, the latch is reset as described above, making pin 6 high again. When 60 nsec elapse after WWL goes high, the low that reset the latch appears at the 60 nsec delay line output (pin 8), resetting latch X39Y29B. After an additional 30 nsec, the pin 8 output of the delay line returns high, completing the cycle. Thus, both latches are statically in a reset state with highs on their D-inputs. WWL clocks both latches, driving UWS (Upper Word Strobe) high and LWS (Lower Word Strobe) low. Sixty nanoseconds later, X39Y29B is reset, making UWS low and LWS high.

AND gate X41Y1D generates two strobes. Statically, this gate's output is high. It goes low initially when X39Y29A's output goes low. After 30 nsec, the latch clears itself, causing its pin 6 output to go high. This causes the AND gate's output to return high. The AND gate's output remains high until the 30 nsec active low pulse reaches the pin 8 output of the delay line. This output causes the AND gate's output to go low for an additional 30 nsec. Thus, the AND gate outputs two 30-nsec active low pulses each time WWL goes high. These strobes are inputs to the Read FIFO Load Decoder.
Read FIFO Load Decoder

The Read FIFO Load Decoder consists of OR gates X37Y9A, X37Y9B and X37Y9C. Two 30-nsec active low strobes are applied to all OR gates after the rising edge of each WWL pulse. During the Sequential Read process, one of these OR gates will have a low input from X39Y9B, the 2- to 4-line decoder that decodes the channel address. This OR gate’s output goes low during each strobe input. FLA, FLB and FLC are the FIFO Load strobes for the Channel A, B and C FIFOs, respectively.

Zoom Factor Load Decoder

The Zoom Factor Load Decoder consists of NOR gates X47Y9D, X14Y15B and X14Y15D. These gates are strobed by SAG/ which is low during the Sequential Read cycles for the first line of a full screen or panel. Therefore, during these lines, ZOC, ZOB and ZOA go high during the Sequential Read cycles for Image 2, Image 1 and the Graphics Channels, respectively.
WIDE WORD Data Latches

The WIDE WORD Data Latches consist of 16 parallel connected D-type latches shown on sheets 11 and 12 of the schematics. Table 21 shows the chip locations, WIDE WORD Data Bus inputs and Memory Data (MD) Bus outputs.

<table>
<thead>
<tr>
<th>Chip</th>
<th>WIDE WORD Input Bits</th>
<th>Memory Data Output Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>X4Y160</td>
<td>WD000-WD070</td>
<td>MD00-MD07</td>
</tr>
<tr>
<td>X2Y160</td>
<td>WD080-WD150</td>
<td>MD08-MD0F</td>
</tr>
<tr>
<td>X4Y149</td>
<td>WD160-WD230</td>
<td>MD10-MD17</td>
</tr>
<tr>
<td>X2Y149</td>
<td>WD240-WD310</td>
<td>MD18-MD1F</td>
</tr>
<tr>
<td>X4Y138</td>
<td>WD320-WD390</td>
<td>MD20-MD27</td>
</tr>
<tr>
<td>X2Y138</td>
<td>WD400-WD470</td>
<td>MD28-MD2F</td>
</tr>
<tr>
<td>X4Y94</td>
<td>WD480-WD550</td>
<td>MD30-MD37</td>
</tr>
<tr>
<td>X2Y94</td>
<td>WD560-WD630</td>
<td>MD38-MD3F</td>
</tr>
<tr>
<td>X4Y127</td>
<td>WD001-WD071</td>
<td>MD40-MD47</td>
</tr>
<tr>
<td>X2Y127</td>
<td>WD081-WD151</td>
<td>MD48-MD4F</td>
</tr>
<tr>
<td>X4Y116</td>
<td>WD161-WD231</td>
<td>MD50-MD57</td>
</tr>
<tr>
<td>X2Y116</td>
<td>WD241-WD311</td>
<td>MD58-MD5F</td>
</tr>
<tr>
<td>X4Y105</td>
<td>WD321-WD391</td>
<td>MD60-MD67</td>
</tr>
<tr>
<td>X2Y105</td>
<td>WD401-WD471</td>
<td>MD68-MD6F</td>
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<td>WD481-WD551</td>
<td>MD70-MD77</td>
</tr>
<tr>
<td>X2Y83</td>
<td>WD561-WD631</td>
<td>MD78-MD7F</td>
</tr>
</tbody>
</table>

Table 21. WIDE WORD Data Latches’ Inputs and Outputs

Each chip is clocked by WWLA or WWLB (WIDE WORD Latch A or B, respectively). These clocks are outputs of line drivers X39Y18C and X39Y18D which are driven by the inverted WDTAC/. Therefore, the WIDE WORD Data Latches are clocked on the leading edge of the WIDE WORD Data Accepted handshake response from the memory.

The outputs of the first eight chips listed in Table 21 are enabled onto the MD bus when LWS goes low; the outputs of the second eight chips are enabled onto the MD bus when UWS goes low. For additional information on LWS and UWS, refer to Timing Diagram 10 on page 5-48 and the Double Strobe Generator description on page 5-48.
Channel A, B and C FIFOs

The Channel A, B and C FIFOs are shown on schematic sheets 14, 16 and 18, respectively. Since the Channel FIFOs are identical, only the Channel A FIFO is described here.

The Channel A FIFO consists of eight cascaded 512-word by 9-bit FIFOs. Because the MSB of each FIFO is unused, the FIFOs function, for loading purposes, as a 512-word by 64-bit FIFO. In an increasing order of significance, the FIFOs are located at: X10Y156, X10Y141, X10Y126, X10Y111, X10Y96, X10Y81, X10Y66 and X10Y51.

The lower 64 bits of the data word are enabled to the FIFO inputs by LWS. Then, these inputs are loaded into the FIFOs by the first 30 nsec FLA strobe (refer to Timing Diagram 10 and the Read FIFO Load Decoder description). After the lower half of the data word is stored, UWS goes low, enabling the upper half of the data word to the FIFO inputs. Finally, the last FLA strobe stores this data in the FIFOs. Note that FLA connects to the Write input (pin 1) of each FIFO via a 47-ohm resistor. The resistors dampen ringing oscillations.

The FIFOs are unloaded individually by BSA0-BSA7 (Byte Select Channel A 0-7). For information on the unload signals, refer to the Pixel Selector description below.

The FIFOs are reset during each vertical blanking period by VG. This ensures that FIFOs do not retain any unread pixels that could occur as a result of a missed read strobe, etc.
Channel A, B and C Pixel Selectors

The Pixel Selectors are shown on schematic sheets 13, 15 and 17 for Channels A, B and C, respectively. Since the selectors are identical, only the Channel A Pixel Selector is described here. Refer to Figures 6 (pages 4-13 and 4-14) and 16 (page 4-52) as necessary.

Zoom FIFO

The Zoom FIFO consists of a 16-word by 4-bit FIFO located at X51Y10. VG holds the FIFO in a reset state during scan lines 0-42. During scan line 43 or if HSL/ goes low, ZOC, ZOB and ZOA are asserted in that order. The positive leading edge of ZOA loads the ZF bus data into the FIFO. In the split panel mode, ZOA is asserted again at the beginning of the Horizontal Switch Line (leading falling edge of HSL/). Thus, the FIFO has two zoom factors loaded into it while HSL/ is asserted.

The first word loaded into an empty or reset FIFO appears on its outputs within a few nanoseconds (fall through time) without receiving an unload pulse. Thus, the zoom factor loaded by ZOA during line 43 appears on the FIFO’s outputs (Q0-Q3) about 25 nsec after the rising edge of ZOA. This zoom factor output remains until the end of the full screen or the upper panel in a split screen display. During a split screen mode, the lower panel’s zoom factor is loaded into the FIFO at the beginning of the HSL/ line as described above. At the end of the HSL/ line, the rising trailing edge of HSL/ unloads the lower panel’s zoom factor. This zoom factor output remains until the end of the lower panel.

Start Address FIFO

The Start Address FIFO consists of the 16-word by 4-bit FIFO located at X51Y28. Loading, unloading and resetting of this FIFO are identical to those inputs in the Zoom FIFO description above.
Zoom Pixel Hold-off Counter

The Zoom Pixel Hold-off Counter is a synchronous 4-bit up/down counter located at X51Y1. This counter is a down counter enabled by DLG/(lines 44-524).

The AND gate located at X47Y1C loads X51Y1 with the output of the Zoom FIFO when either of its inputs go low. The AND gate’s pin 9 input holds the counter in the load state during scan lines 00-43. During scan lines 44-524, the pin 9 input is high. The AND gate’s pin 10 input goes low each time the counter underflows. Thus, during scan lines 44-524, the counter repeatedly loads itself with the Channel A zoom factor, decrements it to zero at the pixel clock rate and reloads itself. Since counter loading is synchronous, the decrement and reload cycle equals the zoom factor plus one clock period.

The RCO output of X51Y1 is ORed with DLG/ by OR gate X51Y55A. This causes the OR gate’s output to be high during vertical and horizontal blanking times. During scanning of the visible pixels, the OR gate’s output goes low each time the zoom factor is decremented to zero (X51Y1’s RCO is low). GLG (Gated Line Gate) is high during the visible pixels. This causes a high output from OR gate X51Y55C during the visible pixel times, enabling the pin 9 input of AND gate X47Y17C. Therefore, during the visible pixel time of lines 44-524, AND gate X47Y55A passes the RCO outputs of X51Y1 to the enable inputs of the Pixel Counter.

Pixel Counter

The Pixel Counter consists of the 4-bit up/down synchronous binary counter located at X51Y46. This counter counts up on the rising edge of PXLCK-P when enabled by AND gate X47Y17C. It is preset to zero at the start of the first visible line of a frame. Thereafter, the counter is controlled by AND gate X47Y17C (described below). The counter’s three LSBs drive X51Y37, the FIFO Read Strobe Decoder. The counter’s QA-QD outputs drive comparator X51Y19, a component of the End/Start Pixel Comparison logic.
The FIFO Read Strobe Decoder consists of a 3- to 8-line decoder located at X51Y37. The decoder outputs are all high when AVR (Channel A FIFO status) is low (empty). When AVR is high (not empty), the decoder is enabled. The A-C inputs determine which of the decoder's Y outputs is low when AVR is high. Table 22 describes the decoder's outputs.

<table>
<thead>
<tr>
<th>C</th>
<th>B</th>
<th>A</th>
<th>AVR</th>
<th>Y7</th>
<th>Y6</th>
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</table>

X = don't care

Table 22. FIFO Read Strobe Decoder Outputs

BSA0-BSA7 (Byte Select Channel A 0-7) are driven by X51Y37's Y0-Y7 outputs, respectively. When a BSA output is low, the respective Channel A FIFO's output is enabled. The trailing rising edge of the BSA signal increments its FIFO's internal read address and tri-states its output.

The End/Start Pixel Comparison and Match Logic consists of a 4-bit comparator located at X51Y19, OR gates X51Y55B and X51Y55C, AND gate X47Y17A and NOR gate X47Y9B. This logic has a Start Address Synchronization phase at the start of each line and a flushing phase at the end of each line. During pixel writing, this logic is ignored by the remainder of the Pixel Selector logic. In the following discussion, assume a zoom factor of 0 and a start address of 8. That is, the frame is roam eight pixels to the right (MA03-MA00 are 1, 0, 0 and 0, respectively).
Just prior to the end of line 43, DVG is still low, presetting the Pixel Counter (X51Y46) to zero. At the beginning of this line, ZOA goes high, loading the pixel start address offset (1000h) into the Start Address FIFO (X51Y28). At the same time, the zoom factor is loaded into X51Y10.

At the start of line 44, DVG goes high, putting the pixel counter in the count mode. Each visible scan begins with 128 blanked pixels that are part of the horizontal blanking period. The End/Start Pixel Comparison and Match Logic executes the Start Address Synchronization phase during this time. The Pixel Counter increments until its output count equals that of the Start Address FIFO. This phase ends when the comparator generates a high at its pin 6 output. The comparator's pin 6 goes high if the A0-A3 inputs match its B0-B3 inputs, respectively, and the A=B input (pin 3) is high.

The A=B input of the comparator goes high each time pixel 0 of a WIDE WORD is addressed. The following gates control the A=B input of the comparator:

- AND gate X47Y17A
- OR gate X51Y55B
- NOR gate X47Y9B

Prior to retrieving the first line of a frame, DVG presets the Pixel Counter to zero (described above). At the end of each line, the End/Start Pixel Comparison and Match Logic flushes any unused pixels in the last WIDE WORD of the line. The flushing cycle ends when the Pixel Counter's address rolls over to zero (described below). Therefore, the Pixel Counter is always at address zero prior to the beginning of the Start Address Synchronization Phase. Thus, the Y0 output of X51Y37 and the QD output of the Pixel Counter are both low, causing a high output from NOR gate X47Y9B. A high output from the NOR gate forces a high output from OR gate X51Y55B and a high input to the A=B input of the comparator and pin 2 of AND gate X47Y17A.

During horizontal blanking, LG/ is high. Therefore, a high from OR gate X51Y55B causes the AND gate's output to go high. AND gate X47Y17A and OR gate X51Y55B form a self latch, latching the output of the NOR gate until LG/ goes low. This latched high output from the NOR gate means the Start Address Synchronization phase is in progress. When LG/ is high and the NOR gate's output is low, the flushing phase is in progress.
Unequal A and B inputs to the comparator cause the pin 6 output of
the comparator and the pin 10 input of OR gate X51Y55C to be low.
GLG, this OR gate's pin 9 input, is high only during the visible pixels
of lines 44-524. Thus, GLG is low during both phases. Therefore,
unequal A and B inputs (A=8, B=0) cause OR gate X51Y55C's output
to be low. This causes a low output of AND gate X51Y46, enabling
the Pixel Counter.

The Pixel Counter increments on the rising edge of every pixel clock
(PXLCK-P) if AND gate X47Y17C's output is low. After eight
PXLCK-P pulses, the Pixel Counter's output equals 8 and matches
that of the Start Address FIFO, causing pin 6 of the comparator to go
high. This drives the output of OR gate X51Y55C high, causing the
output of AND gate X47Y17C to go high. At this time, Pixel Counter
incrementing is inhibited and the Pixel Counter is synchronized to
the Start Address FIFO output.

At pixel 128, GLG goes high, driving pin 9 of AND gate X47Y17C high
regardless of the pin 6 output of the comparator. At the same time,
LG/ goes low, releasing the latch consisting of AND gate X47Y17A
and OR gate X51Y55B. Throughout the next 640 pixel clocks, the
Pixel Counter increments only when enabled by the RCO output of
the Zoom Pixel Hold-off Counter (via OR gate X51Y55A).

Assuming a zoom factor of 0 and a start address offset of 8, the Pixel
Counter has an address output of 8 at the end of the visible portion of
the scan line (pointing at the ninth pixel of the 41st WIDE WORD).
At this time, LG/ goes high and the flushing phase begins.

The comparator's A and B inputs match at the beginning of the
flushing phase in this example. Because the 3 LSB outputs of the
Pixel Counter are low, the Y0 output of the FIFO Read Strobe
Decoder is low. However, the MSB output of the Pixel Counter is
high, resulting in a low output from the NOR gate. Thus, the A=B
input of the comparator is low, forcing the pin 6 output of the
comparator low.

Because GLG is also low at this time, OR gate X51Y55C's output is
low, causing AND gate X47Y17C's output to go low. This enables the
Pixel Counter. After the Pixel Counter's eighth increment, its output
address is zero. At this time, the Pixel Counter's QD output to pin 6
of the NOR gate and the FIFO Read Strobe Decoder's Y0 output to
pin 5 of the NOR gate are low, causing the NOR gate's output to go
high. The high output from the NOR gate is latched by AND gate
X47Y17A and OR gate X51Y55B. This completes the flushing phase.
At this time, the Pixel Counter's output address is zero, the A=B
input of the comparator is high and the pin 6 output of the
comparator is low. This is also the beginning of the next Start
Address Synchronization phase.
Screen Control Section

The Screen Control Section consists of the:

- Horizontal and Vertical Panel Switch Generators
- Display Control (A Board Mode Controls)

The Horizontal Panel Switch Generator is shown on sheet 10 of the schematics; the Vertical Panel Switch Generator and Display Control are shown on sheet 19.

Horizontal Panel Switch Generator

The Horizontal Panel Switch Generator consists of:

- an 8-bit synchronous up/down counter located at X41Y58
- a 4-bit synchronous up/down counter located at X39Y37
- a 10-bit D-type latch located at X39Y62

The counters are cascaded to form a 12-bit down counter that functions as a 10-bit down counter because the two MSBs (C and D inputs of X39Y37) are grounded.

When a binary down counter decrements through zero, all Q outputs go high (minus one). A 10-bit binary counter has a count range of 0000 - 1023p. Since the maximum count required is 639D, 10 bits are more than enough for horizontal pixel counting. Therefore, the 2 MSB outputs of X39Y37 can be used for other purposes. These bits go low during counter loading and only go high when the counter decrements through zero.

The memory mapped latch is loaded with the split pixel address on the rising edge of PSHL (Panel Switch Horizontal Load). DLG presets the counter to the output of this latch during the horizontal blanking of lines 44-524. DLG is high during the 640 visible pixels of lines 44-524, allowing the counters to decrement on the rising edge of PXLCK-M.
When X41Y58 decrements to zero, its TC (Terminal Count) output goes low, enabling X39Y37. The next rising edge of PXLCK-M decrements X41Y58 to minus one (11111111B) and decrements X39Y37. When both counters reach zero, the next clock pulse decrements them to minus one. This disables additional counting because the QD output of X39Y37 drives the CEP and CET inputs of X41Y58 high. At this time, LRS (Left/Right Switch) goes high and remains high for the remaining visible pixels. Thus, LRS is low while scanning pixels left of the split and high while scanning pixels right of the split.

**Vertical Panel Switch Generator**

The Vertical Panel Switch Generator consists of:

- part of PAL A9 located at X43Y93
- an 8-bit synchronous up/down counter located at X45Y93
- a 10-bit D-type latch located at X47Y93

PAL A9, functioning as the MSB, and X45Y93 form a 9-bit cascaded down counter. The PAL also contains the generator's output signal drivers and logic.

FD00-FD08 are latched into X47Y93 on the rising edge of PVSL (Panel Vertical Switch Load). VG presets X45Y93 with the latch's 8 LSB outputs during vertical blanking. VG also presets the counter's MSB stage with the Q9 output of the latch.

The MSB of the generator (part of PAL A9) consists of a D-type latch with load, hold and count logic driving its D-input. The latch is set to the Q9 output of X47Y93 on the rising edge of LG/ when VG is low (during vertical blanking). During visible line scanning, the MSB either toggles to its opposite state or holds its present state. Holding occurs if the TC output of X45Y93 is high; toggling occurs if the TC output of X45Y93 is low.

TBG (Top/Bottom Gate) is the output of a self latch that goes high when the 9-bit counter underflows and remains set until VG goes low. Thus, TBG is low above the horizontal split line and high below it. DTB (Delayed Top/Bottom) is TBG ANDed with the Q4 output of X43Y82. This output is high any time horizontal panels are displayed. HSL/ (Horizontal Switch Line) is low only during the scan line that causes the counter to underflow. Also, the Q4 output of X43Y82 must be high to qualify this signal.
While not actually a part of the Vertical Panel Switch Generator, the 8-bit comparator located at X45Y82 on sheet 19 of the schematics is included here because it is driven exclusively by the generator's outputs. The comparator detects the first line of the upper label field when horizontal or quad panels are displayed. The label field for the upper panel is the last 9 lines of the panel. The comparator compares the 8 LSB outputs of the generator (P inputs) to a Q-input value of 00001000B (8 decimal). The comparator is enabled when the MSB of the generator is low. Therefore, the comparator's pin 19 output (LSS/Label Split Start) goes low during the ninth-from-the-last line of the upper panel. This signal is used by the Label Generator.

Display Control

The Display Control section consists of three octal D-type latches located at X43Y82, X39Y90 and X41Y112, and two PALs located at X43Y93 and X41Y77 (PALs A9 and A10, respectively).

The Display Control section allows the user to define what channel input data (Image 1, Image 2, Graphics or Dual Channel) to display, how to display that data (full screen, split screen or quadrant) and where that data will appear (full screen, left panel, right panel, upper panel, lower panel or one of the quadrants).

Display Mode Control Background

The user controls the display via a 16-bit Display Mode Control word that is intended to be "user friendly." However, it is not directly compatible with other inputs of the Prioritizer, the circuit that controls Dual Channel Multiplexer switching. The Prioritizer deals with several data inputs in addition to image and graphics data. Each of these inputs is a switch type signal, i.e., on a pixel by pixel basis, an asserted input signal indicates that its respective data source wants to drive the pixel. The Display Control section processes the Display Mode Control word into Prioritizer compatible image and graphics switch signals and a 2-bit Mode Control word and sends these signals to the Prioritizer.

The last page of McIDAS Design Note 46, located in the Reference section of this manual, defines the bits of the Display Mode Control word. Bits 0-7 are Image 1 and 2 mask bits; bits 8-B are Graphics mask bits; bits C-E are the Display Mode; bit 15 is the Window Cursor 2 mask bit.
**Channel Mask Bits**

Four mask bits are provided for each channel in the Display Mode Control word. The interpretation of these bits is modified by the Display Mode, i.e., the Display Mode and mask bits are interactive. For each channel, a mask bit is assigned to each display quadrant as shown in Design Note 46. If the Display Mode is Quad Panels, the mask bits indicate which data source drives each quadrant. If the Display Mode is other than Quad Panel, the highest order mask bit of the quadrants composing the panel or full screen is used.

For example, assume the user wants to display Image 2 in the upper horizontal panel and Graphics in the lower horizontal panel. First, the Display Mode is set to Horizontal Panels (bit D is high, bits C and E are low). Next, an Image 2 and a Graphics mask bit must be selected. Bits 6 and 4 represent the Image 2 upper left and upper right quadrants, respectively; bits 9 and 8 represent the lower left and lower right Graphics quadrants, respectively. Therefore, bits 6 and 9 of the Display Control word are set because bit 6 represents the highest Image 2 quadrant in the upper horizontal panel and bit 9 represents the highest Graphics quadrant in the lower horizontal panel.

**Display Mode Bits**

As indicated in Design Note 46, FD0E, FD0D and FD0C define the Display Mode. Table 23 on page 5-63 shows the binary code for each mode.

Mode 0 allows the user to select one of the available data sources (i.e., Image 1, Image 2, Dual Channel or Graphics) to be displayed on the Dual Channel.

Mode 1 allows the user to select any two of the four data types (a different data source for each horizontal panel).

Mode 2 is similar to Mode 1, except the panels are oriented vertically rather than horizontally.

Mode 3 allows the user to display all four data types simultaneously, with a different type in each quadrant.

Mode 4 is a full screen mode in which Image 1 and Image 2 are shown on alternate fields with the images alternating every 1/60 second. The resulting display is called Alternate Frame Stereo.

Mode 5 is a composite of Modes 1 and 4. It allows the user to select the upper or lower horizontal panel for Alternate Frame Stereo and display any of the four data types on the other.
Mode 6 allows the user to display an image frame on the Graphics Channel. This is possible because there are no hardware differences between the graphics and image channels from the Dual Channel Multiplexer’s perspective. In this mode, three video channels are displayed. Images 1 and 2 are displayed on the Image 1 and Image 2 monitors, respectively; Image 3 is shown on the Dual Channel’s monitor. However, limitations are introduced when no channel is dedicated to graphics. For example, no channel can have a graphics overlay since the graphics channel is displaying an image. Any required graphics (e.g., geographical boundaries, pressure contours, etc.) must be embedded by the host before downloading to the workstation.

Mode 7 is a combination of Modes 1 and 6. The upper or lower horizontal panel displays the third image processed by the Graphics Channel, while the remaining horizontal panel displays any one of the data sources named in Mode 0 except Graphics.

Display Mode Control
Circuit Description

Control of the Dual Channel display is via the 16-bit Display Mode Control word written to address C00E00H. Writing to this address asserts PMSL (Panel/Mask Select Load). The rising trailing edge of PMSL latches the lower and upper bytes of the control word into octal latches located at X39Y90 and X43Y82, respectively. PALs A9 (partial) and A10 process the latched Display Mode Control word into I1 (Image 1), I2 (Image 2) and W (Graphics) switch signals, and Mode Controls MC1 and MC0.

The I1 and I2 drive signals are resynchronized to PXLCK-F by D-type latch X41Y112. The W drive is also resynchronized by X41Y112, but is delayed one extra clock period to compensate for differences in processing between the I and W drive signals. These differences occur because the I drive signals are latched outputs of PAL A10 and the W drive signal is a combinatorial output of PAL A9. The internal latching of the I drive signals delays them one clock period before they reach latch X41Y112.

The I1, I2 and W outputs of latch X41Y112 are switch signals that indicate Image 1, Image 2 or Graphics, respectively. The I1, I2 and W outputs are summarized in Table 10 on page 4-58. In the example above, I2 is high above the horizontal split line; W is high below the horizontal split line; I1 is low in both panels.

The PALs require panel switching inputs in addition to the Display Mode word (TBG and LRS) to enable and disable the I1, I2 and W signals at the desired scan line and pixel. For additional information on the I and W signals, refer to the PAL A9 and A10 equations in the Reference section of this manual.
MC1 (MSB) and MC0 (LSB), the Mode Control outputs of PAL A9, are derived from the Display Mode portion of the Display Mode Control word and OEF. OEF toggles at the frame rate and is used in generating the stereo mode codes.

The presence or absence of certain data sources affects the Prioritizer as a function of the Mode Control. For example, if Graphics is not enabled (W is low) and the Mode Control is zero, Graphics will not be enabled to the Dual Channel. However, if the Mode Control is 3, the Graphics Channel is enabled to the Dual Channel regardless of W. The Prioritizer uses the Mode Control bits in each of its output equations. For more information on MC1 and MC0, refer to the Prioritizer Output Signals description. Table 23 below shows the Display Mode to Mode Control mapping.

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<tr>
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<th>Display Mode</th>
<th>MC1</th>
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<th>Output Mode Control</th>
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*Toggled at the vertical field rate (1/60 sec) by OEF (Odd/Even Field)

Table 23. Display Mode to Mode Control Mapping
Prioritizer

The Prioritizer consists of PAL A11 located at X39Y101 and is shown on sheet 20 of the A Board schematics. The PAL equations for A11 are listed in the Reference section of this manual. Those equations are reprinted in this section for your convenience.

A11 is described by analyzing the set of equations for each output. The outputs of A11 drive the Image 1, Image 2 and Dual Channel Multiplexers via the D-type latches at X41Y101 and X41Y112. These latches resynchronize the output drives with PXLCK-F and introduce a resynchronization delay that realigns the Prioritizer’s output drives with the data type transitions.

The Prioritizer:

- resolves data contention
- selects default data sources for each channel

Priority Resolution

The Prioritizer resolves contention when more than one data source competes for the same pixel. For example, it’s possible for one of the cursors, the Graphics Channel and one of the image channels to simultaneously attempt to write to a given Dual Channel pixel. The Prioritizer enables the highest priority data source. In this example, the cursor is gated through the Dual Channel’s multiplexer.

Default Data Source Selection

In addition to priority resolution, the Prioritizer has built-in default conditions that allow it to select a default data source for each channel. For example, the outputs of Image 1, Image 2, the Graphics Channel and the Dual Channel are inputs to the Dual Channel Multiplexer. The Prioritizer must select one of these data sources to be displayed on the Dual Channel monitor. If only Image 1 is enabled, the Prioritizer automatically selects Image 1 as the drive source for the Dual Channel Output. If all data sources are active, the Dual Channel palette’s output drives the Dual Channel Multiplexer.
Prioritizer Inputs

Several Prioritizer inputs were described in the previous Mode Control section. They include:

- Image Controls I1 and I2
- Mode Controls MC0 and MC1
- Graphics Control W

Additional Prioritizer inputs consist of:

- Graphics Channel outputs
- Cursor Generator outputs
- Label Blanking
- Character Generator output
- Window Cursor 2

These inputs are described below.

Graphics Channel Outputs

Graphics in the workstation provide charts, graphs, state and international boundary overlays, etc. Boundary maps and most chart overlays (e.g., pressure contours, etc.) are usually used in conjunction with a specific image. To accommodate this, the Graphics Channel is divided in half. The lower half (bits 0-3) is used with Image 1; the upper half (bits 4-7) is used with Image 2.

The Graphics Channel is bit mapped, i.e., the user assigns a particular graphics overlay to a bit plane. For example, the user can assign the map of the United States to bit 0 and a pressure contour to bit 1 of each Graphics Channel byte. It's possible to use a single bit from each graphics byte to generate a graph or map because graphics do not contain intensity information. On a pixel by pixel basis, graphics are either on or off. Therefore, up to four graphs can be associated with each image in the Dual Channel or stereo modes. The Prioritizer needs to know if any bit plane associated with a particular image channel is active. For this reason, the output of the Masked Graphics Latch is applied to the Prioritizer.

Refer to sheet 20 of the A Board schematics. GRA0-GRA3 are the graphics bits associated with Image 1; GRA4-GRA7 are the graphics bits associated with Image 2. These groups of bits are NORed together by NOR gates X47Y106A and X47Y106B, respectively. The outputs of these gates are control inputs to A11. They go low if one or more of their respective inputs go high.
Cursor Generator Outputs

GCUR0 and GCUR1 are the latched and masked outputs of Cursor Generators 0 and 1, respectively. When one of these bits is high, the respective cursor is masked on and the pixel currently being painted is part of the respective cursor.

Label Blanking

Each channel may have one label field for a full screen mode or two label fields for the horizontal split screen modes (includes Quad Panels). These label fields consist of the last nine horizontal scans in a frame or panel. They may be masked off by outputs of the respective channel's mask latch. PAL A10 produces each label field control signal by combining the respective mask bit (GMA, I1MA, I2MA) with inverted LVB/ (Label Vertical Boundary) and LCL/ (Label Counter Load).

LVB/ and LCL/ are active low outputs of the Character Generator. LVB/ is asserted only during the first horizontal scan line in the label field. LCL/ is asserted for the eight subsequent scan lines of the label field. These signals are ORed together to produce a 9-line label gate which is ANDed with each channel's character generator mask bit to produce the three label field control signals.

Character Generator Output

V0A is the latched output of the Character Generator (see sheet 21). V0A is high when the pixel currently being painted is part of a displayed character in a label.

Window Cursor 2

The WWW's Window Cursor 2 feature allows the user to combine the features of Cursor 1 and Image 2. The result is a moveable window, defined by the Cursor 1 boundary parameters, that shows Image 2 only. This is useful when the user displays stereo or the Dual Channel and wants to observe only the Image 2 component. Window Cursor 2 removes Image 1 within the boundaries of Cursor 1.

WC2 is the latched Window 2 enable mask (see sheet 19). It is NANDed with V09 by X37Y106D. V09 is the latched Cursor Generator 1 output (latched CUR1 - see sheet 21). Thus, the output of X37Y106D goes low if the Window Cursor 2 feature is masked on and pixels within the Cursor 1 boundaries are currently being scanned. The output of the NAND gate is applied to the Prioritizer via the D-type latch located at X25Y86D. This latch delays the leading edge of the Window Cursor 2 control signal to the next rising edge of PXLCK-F, resynchronizing the control signal with its proper Image 2 pixel.
**Prioritizer Output Signals**

The Prioritizer output signals consist of:

- Channel 1 Multiplexer Control signals
- Channel 2 Multiplexer Control signals
- Dual Channel Multiplexer Control signals

**Channel 1 Multiplexer Control Signals**

G11EN/ (Graphics to Image 1 Enable) and IC1EN/ (Image to Channel 1 Enable) are Channel 1 Multiplexer control signals. They originate from A11's pin 16. The latch drive input for IC1EN/ is driven by A11's pin 16. NAND gate X37Y106C, functioning as an inverter, produces the latch drive input for G11EN/ by inverting A11's pin 16 output. Thus, Channel 1 is driven by Image 1 or the Graphics Channel.

The equation for A11’s pin 16 is:

\[
SC1 = \neg L & \neg M1 & MC0 \quad \text{(term 1)} \\
\# \neg L & M1 & \neg MC0 \quad \text{(term 2)} \\
\# GLB & \neg M1 & MC0 \quad \text{(term 3)} \\
\# GLB & M1 & \neg MC0 \quad \text{(term 4)} \\
\# LB1 & \neg V0A \quad \text{(term 5)}
\]

This equation's output (SC1 - pin 16) goes high if any term goes true. Since pin 16 drives IC1EN/, IC1EN/ goes high when SC1 goes high, disabling the Image 1 input and enabling the Graphics Channel input.

The stereo display modes are Mode 1 (MC1 = 0 and MC0 = 1) and Mode 2 (MC1 = 1 and MC0 = 0). Term 1 in the above equation enables lower graphics in Mode 1; term 2 enables lower graphics in Mode 2. Together, they enable graphics if any lower graphics bit is high during stereo displays. Terms 3 and 4 enable the Graphics Channel while scanning the graphics label field in the stereo modes. Term 5 enables the Graphics Channel while scanning the Image 1 label field unless the pixel being painted is part of a displayed character. That is, the Graphics Channel is enabled while painting Image 1's label background.

IC1EN/ enables the Image 1 input to Channel 1's Multiplexer when it is low. The PAL equation for SC1 goes high if any term qualifies. By using DeMorgan's Theorem and various reduction techniques beyond the scope of this manual, an active low equivalent of SC1 can be derived.
The resulting equation is:

\[ \text{!SC1} = \text{!LB1} \& \text{MC1} \& \text{MC0} \quad \text{(term 1)} \\
# \text{V0A} \& \text{MC1} \& \text{MC0} \quad \text{(term 2)} \\
# \text{V0A} \& \text{!MC1} \& \text{!MC0} \quad \text{(term 3)} \\
# \text{!LB1} \& \text{!MC1} \& \text{!MC0} \quad \text{(term 4)} \\
# \text{!GLB} \& \text{V0A} \& \text{LG} \quad \text{(term 5)} \\
# \text{!GLB} \& \text{LB1} \& \text{LG} \quad \text{(term 6)} \]

Terms 1 and 2 enable Image 1 in Display Mode 3 while painting Image 1 or character pixels in the Image 1 label field. In Mode 3, the Graphics Channel is enabled while painting Image 1's label background. At all other times, while in Display Mode 3, the Image 1 input to Channel 1's multiplexer is enabled. Term 3 enables Image 1 while painting an Image 1 character pixel in Display Mode 0. Term 4 disables Image 1 in Display Mode 0 while Image 1 label background pixels are painted. Together, terms 5 and 6 enable Image 1 when writing to an Image 1 character pixel except when the pixel is also a lower graphics, or an Image 1 or Graphics Channel label background.

CLRGI/ (Clear Graphics to Image 1 and 2) is also a Channel 1 Multiplexer control signal. It is output directly from pin 23 of PAL A11. CLRGI/ drives the Clear pins low on the Graphics Channel portion of the Channel 1 Multiplexer in Display Mode 3 (see sheet 31 of the A Board schematics). Since the only time graphics are enabled in Display Mode 3 is while painting Graphics label background pixels, the sole purpose of CLRGI/ is to blank the Graphics label background. The equation for CLRGI/ is: \( \text{!CLI} = \text{MC1} \& \text{MC0} \) (Display Mode 3)

Channel 2 Multiplexer Control Signals

G12EN/ (Graphics to Image 2 Enable) and IC2EN/ (Image to Channel 2 Enable) are the Channel 2 Multiplexer control signals. They are functionally identical to G11EN/ and IC1EN/, respectively. Refer to the G11EN/ and IC1EN/ descriptions above for more information.

Channels 1 and 2 Summary

Each channel's multiplexer receives data from its respective image channel and the Graphics Channel. The image channel drives its multiplexer at all times except when the pixel is a label background or a graphics pixel. Graphics are allowed during Display Modes 1 and 2 (stereo modes) only. Characters are painted by the channel they represent. The Graphics Channel paints all label background pixels.

Channels 1 and 2 data in decreasing priority are:

- label characters (highest)
- label background
- graphics
- image (lowest)
The Dual Channel Multiplexer control signals are:

- I1DCEN/ (Image 1 to Dual Channel Enable)
- I2DCEN/ (Image 2 to Dual Channel Enable)
- DCEN/ (Dual Channel Enable)
- GDCEN/ (Graphics to Dual Channel Enable)
- CLRGDC/ (Clear Graphics to Dual Channel)

Each of these signals is described below.

I1DCEN/

I1DCEN/ is the pin 12 output of D-type latch X41Y101. The input for this latch (pin 13) is driven by PAL A 11's pin 18. The PAL equations for this PAL generate a high output. Since the multiplexer requires a low signal to gate Image 1 to the Dual Channel DAC, all ORed terms must be false simultaneously to assert I1DCEN/. The equation for I1DCEN/ is:

\[
\text{DC1} = \begin{array}{c}
\text{MC1} \\
# \ CB1 & !MC1 & !MC0 \\
# \ CB2 & !MC1 & !MC0 \\
# \ !WC2 & !MC1 & !MC0 \\
# \ !LG & W & !MC1 \\
# \ !UG & W & !MC1 & !MC0 \\
# \ \text{GLB} \\
# \ !I2 & !MC1 & !MC0 \\
# \ !I1 & !I2 & !MC1 & !MC0
\end{array} \quad (\text{Term 1-9})
\]

Term 1 is false during Display Modes 0 and 1. Terms 2 and 3 are false if neither Cursor Generator is currently scanning a cursor pixel while in Display Mode 0. Term 4 is false if there is no Window Cursor 2 while in Display Mode 0. Terms 5 and 6 are false if there are no graphics bits (upper or lower) in Display Mode 0, or lower graphics in Display Mode 1. Term 7 is false except while scanning pixels in the Graphics label field. Terms 8 and 9 are false when I1 is high, I2 is low and the Display Mode is 0. That is, if Image 1 is the only active image channel in Display Mode 0, and terms 1-7 are false, Image 1 is displayed on the Dual Channel monitor.
I2DCEN/ 
I2DCEN/ is the pin 9 output of D-type latch X41Y101. The input for this latch (pin 8) is driven by PAL A 11's pin 19. The PAL equations for this PAL generate a high output. Since the multiplexer requires a low signal to gate Image 2 to the Dual Channel DAC, all ORed terms must be false simultaneously to assert I2DCEN/. The equation for I2DCEN/ is:

\[
DC2 = MC0 + CB0 \& \neg MC1 \& \neg MC0 \quad \text{(Term 1)} \\
# CB1 \& \neg MC1 \& \neg MC0 \quad \text{(Term 2)} \\
# \neg LG \& W \& \neg MC1 \& \neg MC0 \quad \text{(Term 3)} \\
# \neg UG \& W \& \neg MC0 \quad \text{(Term 4)} \\
# GLB \quad \text{(Term 5)} \\
# \neg I1 \& \neg I2 \& WC2 \& MC1 \& MC0 \quad \text{(Term 6)} \\
# I1 \& WC2 \& MC1 \& MC0 \quad \text{(Term 7)} \\
# I1 \& WC2 \& MC1 \& MC0 \quad \text{(Term 8)}
\]

The first term restricts the Image 2 drive into the Dual Channel to Display Modes 0 and 2. Terms 2 and 3 are both false unless scanning a cursor pixel in Display Mode 0. Terms 4 and 5 are both false if there are no graphics in Display Mode 0. In addition, no upper graphics are allowed in Display Mode 2 (stereo). Term 6 is false except while scanning a graphics label field pixel. Terms 7 and 8 are simultaneously false when the Display Mode is 0 and the pixel is a Window Cursor 2 pixel, or the Display Mode is 0, the pixel is not a Window Cursor 2 pixel and Image 2 is the only active image channel.

DCEN/ 
DCEN/ is the pin 6 output of D-type latch X41Y101. The input for this latch (pin 7) is driven by PAL A 11's pin 20. The PAL equations for this PAL generate a high output. Since the multiplexer requires a low signal to gate the Dual Channel to the Dual Channel DAC, all ORed terms must be false simultaneously to assert DCEN/. The equation for DCEN/ is:

\[
DCE = MC1 + MC0 \quad \text{(Term 1)} \\
# CB0 \quad \text{(Term 2)} \\
# CB1 \quad \text{(Term 3)} \\
# WC2 \quad \text{(Term 4)} \\
# \neg LG \& W \quad \text{(Term 5)} \\
# \neg UG \& W \quad \text{(Term 6)} \\
# \neg I1 \quad \text{(Term 7)} \\
# \neg I2 \quad \text{(Term 8)}
\]

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Terms 1 and 2 restrict DCEN/ to Display Mode 0 only. Terms 3 and 4 are simultaneously false if neither cursor generator is currently scanning a cursor pixel. Term 5 is false if the pixel is not a Window Cursor 2 pixel. Terms 6 and 7 are simultaneously false if no graphics bits are high. Terms 8 and 9 are simultaneously false if both image channels are active. Thus, the Dual Channel input is enabled on a pixel by pixel basis if:

- the Display Mode is 0, and
- both image channels are active, and
- the pixel is not a graphics, Widow Cursor 2 or cursor pixel, and
- the pixel is not a Graphics label field pixel.

GDCEN/

GDCEN/ is the pin 15 output of D-type latch X41Y101. The input for this latch (pin 14) is driven by PAL A 11’s pin 17. Pin 17's output goes low and enables graphics to the Dual Channel if any term goes true. The equation for 12DCEN/ is:

\[
\begin{align*}
!GDE & = !LG \& W \& !MC1 \\
& \quad !UG \& W \& !MC0 \\
& \quad CB0 \& !MC1 \& !MC0 \\
& \quad CB1 \& !MC1 \& !MC0 \\
& \quad GLB \\
& \quad !II2 \& !I1 \& !MC1 \& !MC0 \\
& \quad MC1 \& MC0
\end{align*}
\]

(Term 1) (Term 2) (Term 3) (Term 4) (Term 5) (Term 6) (Term 7)

Display Modes 1 (MC1 = 0, MC0 = 1) and 2 (MC1 = 1 and MC0 = 0) are the stereo modes. In stereo, these modes alternate at the field rate (1/60 second). The first term sends lower graphics to the Dual Channel during Display Modes 0 and 1; the second term sends graphics to the Dual Channel during Display Modes 0 and 2. Combined, the first two terms enable upper and lower graphics in Display Mode 0, and enable lower and upper graphics in stereo Display Modes 1 and 2, respectively.

Terms 3 and 4 enable graphics when a cursor pixel is scanned. Term 5 enables graphics when scanning the Graphics label field. Term 6 enables graphics to the Dual Channel in Display Mode 0 when no image channels are active. Term 7 enables the Graphics Channel input to the Dual Channel during Display Mode 3. Display Mode 3 allows the Graphics Channel to function as a third image channel. In this mode, Image 1 goes to Channel 1, Image 2 goes to Channel 2 and Graphics (image 3) goes to the Dual Channel.
CLRGDC/

CLRGDC/ is the pin 2 output of D-type latch X41Y112. The input for this latch (pin 3) is driven by PAL A 11’s pin 22. Pin 22’s output goes low and clears the Graphics Channel outputs to the Dual Channel if any term goes true. The equation for CLRGDC/ is:

!CLD = !LCG & GLB & MC1 & MC0  \hspace{1cm} \text{(Term 1)}
# !CB0 & !W & !I1 & !I2 & !MC1 & !MC0  \hspace{1cm} \text{(Term 2)}
# !CB1 & !W & !I1 & !I2 & !MC1 & !MC0  \hspace{1cm} \text{(Term 3)}

The first term is used in Display Mode 3 only. It is true only during the Graphics label field when the Character Generator is not painting a character pixel. That is, it blanks the Graphics label field background pixels. Terms 2 and 3 clear the Dual Channel in Display Mode 0 when there is no image, graphics or cursor data. By default, the Graphics Channel drives the Dual Channel in the absence of image data. Terms 2 and 3 blank the Dual Channel display if graphics is not enabled (W is low).

\textbf{Dual Channel Summary}

If only one image channel is active, that channel drives the Dual Channel in Display Mode 0 except when scanning a graphics label or label background, cursor, Window Cursor 2 or graphics pixel. During all but the Window Cursor 2 exceptions, the Graphics Channel drives the Dual Channel. Image 2 drives the Dual Channel while Window Cursor 2 pixels are scanned. When both image channels are active, the output of the Dual Channel Palette drives the Dual Channel. During Display Mode 1 (stereo), Image 1 drives the Dual Channel except while scanning lower graphics pixels. The Graphics Channel drives the Dual Channel if one or more lower graphics bits are high.

During Display Mode 2, Image 2 drives the Dual Channel except while scanning upper graphics pixels. The Graphics Channel drives the Dual Channel if one or more upper graphics bits are high. During Display Mode 3, only the Graphics Channel drives the Dual Channel. During this mode, the Graphics Channel acts as a third image channel.
Lookup Tables Section

The Lookup section of the A Board consists of the functional blocks on sheet 2 of Figure 6 (page 4-14). This section consists of Image Channels 1 and 2, the Graphics Channel and the Interlaced Dual Channel. Image Channels 1 and 2 are electrically identical. The Graphics Channel terminates at the input of the Dual Channel Multiplexer. Up to this multiplexer, the Graphics Channel is identical to the image channels. Thus, of these three channels, only Image Channel 1 is described in detail here. Then the Dual Channel is described, followed by the Interlaced Dual Channel.

Image Channel 1

Image Channel 1 consists of:

- Image 1 Data Latch
- Image 1 Mask Latch
- Image 1 Mask Gates
- Masked Image 1 Latch
- Image 1 Palette Load Address Buffers
- Image 1 Palette RAM
- Channel 1 Multiplexer
- Channel 1 DAC
- Channel 1 Sync Driver

Two blocks in the Lookup Tables section provide inputs to one or more channels. They are the Cursor/Blink/Character Latch and the Video Blanking Generator. In the following description, these blocks are described prior to describing the block that uses their outputs.

The Image Channel 1 Data Latch consists of the octal D-type latch located at X20/Y92; it is shown on sheet 23 of the schematics. Clocked by PXLCK-D, it latches V1B0-V1B7 (Video Channel 1 Bus 0-7), resynchronizing the output of the Channel B FIFO with the pixel clock. The latch’s output (V10-V17) is parallel connected to the Image 1 and Dual Channel Mask Gates (refer to sheets 23 and 27, respectively). Only the Image 1 and Image 2 Data Latches drive the Dual Channel Mask Gates. The Graphics Data Latch drives only the Graphics Mask Gates.
The Cursor/Blink/Character Latch consists of the D-type octal latch located at X35Y84; it is shown on sheet 21 of the schematics. PXLCK-F clocks the latch, resynchronizing the input data to the pixel clock's rising edge. VG enables the latch's outputs during scanning of the visible lines. V08-V0B are latched CUR0, CUR1, CHGN and BINK, respectively. They are inputs to the Graphics, Image 1 and Image 2 Mask gates (see schematic sheets 21, 23 and 25).

Image 1 Mask Latch

The Graphics Channel, Image Channel 1 and Image Channel 2 are driven by 12-bit buses. The 8 LSBs of the respective bus are driven by the channel's Data Latch; the 4 MSBs of the respective bus are driven by the outputs of the Cursor/Blink/Character Latch. The channel mask gates allow the user to block bus bits on a bit-by-bit basis via 16-bit mask words. The PS/2 writes these mask words to the respective Channel Mask Latch.

The Image 1 Mask Latch consists of two octal D-type latches located at X23Y103 (least significant byte) and X20Y103 (most significant byte). These latches are shown on sheet 23 of the schematics. I1M0-I1M7 (Image 1 Mask 0-7) are mask bits for V1B0-V1B7, respectively. I1M8-I1MB are mask bits for CUR0, CUR1, CHGN and BINK, respectively. I1MC-I1MF are panel blanking mask bits.

Video Blanking Generator

The Video Blanking Generator consists of PAL A12 located at X23Y92; it is shown on schematic sheets 21, 23 and 25 (partials on each sheet).

The four MSB output bits from X20Y103, a part of the Image 1 Mask Latch, allow the user to blank one or more panels of Channel 1's image data. The Video Blanking Generator uses TBG and LRS for panel switch point information. Table 24 on the adjacent page shows the various blanking possibilities. Because Image 1 data is also an input to the Dual Channel, interpretation of the panel mask output bits is affected by the Dual Channel's Display Mode. Table 24 shows the panel mask bit effects on Image 1 and the Dual Channel (all modes).

The pin 12 output of X23Y92 is the Image 1 blanking signal. This output is resynchronized to the pixel clock by section F of a D-type latch located at X25Y86F. VB1 (Video Blanking - Channel 1) is the resynchronized panel mask output.
### Lookup Tables Section

<table>
<thead>
<tr>
<th>TBG</th>
<th>LRS</th>
<th>Mask Bit</th>
<th>Blanking</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>None</td>
<td>No blanking</td>
</tr>
<tr>
<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
<td>II1MC</td>
<td>Upper panel in Horizontal Panels</td>
</tr>
<tr>
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<td>0</td>
<td>II1ME</td>
<td>Full screen in Full Screen modes</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>II1ME</td>
<td>Left panel in Vertical Panels *</td>
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<td>0</td>
<td>II1MC, II1ME</td>
<td>Full screen in Full Screen modes</td>
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<td>0</td>
<td>II1MC, II1ME</td>
<td>Upper panel in Horizontal Panels</td>
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<tr>
<td>0</td>
<td>0</td>
<td>II1MC, II1ME</td>
<td>Left panel in Vertical Panel *</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>II1MC, II1ME</td>
<td>All but lower right in Quad *</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>II1MC</td>
<td>Full screen in Full Screen modes</td>
</tr>
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<td>1</td>
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<td>II1MF Full screen in Full Screen modes</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>II1MC, II1ME</td>
<td>II1MF All but lower left in Quad *</td>
</tr>
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<td>0</td>
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<td>1</td>
<td>II1MD, II1MF</td>
<td>All but upper left in Quad *</td>
</tr>
</tbody>
</table>

*Applies to Dual Channel Display only. This effect is a combination of Prioritizer panel switching and the Video Blanking Generator.

### Image 1 Mask Gates

The Image 1 Mask Gates allow the user to block Channel 1 image data, and CUR0, CUR1, CHGN or BINK on a bit-by-bit basis. The gates are controlled by outputs of the Image 1 Mask Latch. Refer to the Image 1 Mask Latch description on the previous page for mask information.
The Image 1 Mask Gates consist of eight 3-input AND gates and four 2-input AND gates. These gates are shown on sheet 23 of the schematics. The 3-input AND gates are used for Channel 1 image data bit masking. Each gate passes its respective data bit if its mask bit and VB1 are high. The 2-input AND gates are used for masking the outputs of the Cursor/Blink/Character Latch. Each of these gates passes its respective bit if its mask bit input is high. Note that VB1 is not an input to the 2-input AND gates.

Masked Image 1 Latch

Each channel's mask gates drive a Masked Channel Latch. The Masked Image 1 Latch consists of two cascaded D-type latches located at X20Y54 (latches the masked Image 1 video bits) and X23Y54 (latches the masked Cursor/Blink/Character Latch bits). These tri-state latches resynchronize the data to the rising edge of PXLCK-E. They also function as part of a multiplexer consisting of the Image 1 Palette Load Address Buffers and the Masked Image 1 Latch. The Masked Image 1 Latch is enabled during the visible scan lines by DVG/. The 12 output bits drive the 12 address inputs of the Image 1 Palette RAM.

Image 1 Palette Load Address Buffers

The Image 1 Palette Load Address Buffers allow the PS/2 to address the Image 1 Palette RAM during vertical blanking. Together with the Masked Image 1 Latch, they also form an address multiplexer for the Image 1 Palette RAM.

The Image 1 Palette Load Address Buffers consist of two octal line drivers located at X20Y65 (eight LSBs) and X23Y65; they are shown on sheet 23 of the schematics.

Image 1 Palette RAM

The Image 1 Palette RAM consists of six cascaded, dual ported, 4K by 4-bit static RAMs. They are shown on sheet 24 of the schematics and are located at X31Y158, X31Y145, X28Y158, X28Y145, X25Y158 and X25Y145.

Because the RAMs are dual ported, their D inputs are driven directly by the FD bus. All 24 bits on the FD bus are written into the RAMs when WEI1/(Write Enable Image 1) goes low. This signal is an output of the Memory Mapped Control logic.

The 24 output bits of the Image 1 Palette RAMs are divided into eight bits each of red, green and blue. RAMs X31Y158 and X31Y145 drive the Image 1 Red bus (I1R0-I1R7); RAMs X28Y158 and X28Y145 drive the Image 1 Green bus (I1G0-I1G7); RAMs X25Y158 and X25Y145 drive the Image 1 Blue bus (I1B0-I1B7). During programming, FD00-FD07 provide red bus lookup data; FD08-FD0F provide green bus lookup data; FD10-FD17 provide blue bus lookup data.
Channel 1 Multiplexer

The RGB outputs of the Graphics Channel and Image Channel 1 drive the Channel 1 Multiplexer.

The Channel 1 Multiplexer consists of two sets of tri-state D-type octal latches, one set for each data source. Each set has three latches. The Image 1 latch set consists of X31Y134, X28Y134 and X25Y134. These latches are shown on sheet 24 of the schematics. The Graphics latch set consists of X39Y158, X39Y145 and X39Y132. These latches are shown on sheet 31 of the schematics.

Each latch set resynchronizes its respective data input by latching its data on the rising edge of the pixel clock. The tri-state control for each latch set is driven by the Prioritizer. In addition, the latch sets driven by the Graphics Channel contain a Clear input (CLR - pin 1). Refer to the Prioritizer description (starting on page 5-64) for information on all multiplexer control signals.

Channel 1 DAC

The Channel 1 DAC is located at X48Y150; the Channel 2 DAC is located at X56Y150. Both are shown on sheet 31 of the schematics.

Each channel output DAC converts the three sets of 8-bit binary RGB inputs to these three analog RGB outputs: RI1, GI1 and BI1 (Red Image 1, Green Image 1 and Blue Image 1, respectively). Each analog output drives a doubly-terminated 75-ohm coax cable with a peak to peak voltage of 0.714 volts.

The rising edge of PXLCK-J latches the 24 binary inputs, SYNC/ and BLANK/. If BLANK/ is asserted (low), RI1, GI1 and BI1 are driven to the blanking reference (0 volts) and the binary inputs are ignored. Because SYNC/ does not override any other input, it is asserted only during blanking. When SYNC/ is low, a constant current source on the ISYNC output is switched off. ISYNC can be connected to GI1 via a jumper when using a monitor capable of using a sync encoded green analog input instead of a separate sync input. For more information on the DAC, refer to the BT101 description in the Brooktree PRODUCT DATABOOK.

Channel 1 Sync Driver

The Channel 1 Sync Driver is located at X53Y120A; it is shown on sheet 31 of the schematics. The line driver converts the TTL SYNC/ input to a doubly-terminated 75-ohm coax output. SI1 (Sync Image 1) connects to the BNC connector panel via pin 4 of the VP (Video Port) coax ribbon cable connector.

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Dual Channel

The Dual Channel is driven by the latched outputs of the Channel 1 and Channel 2 Latches. This channel begins with the Dual Channel Mask Latches and the Dual Channel Mask Gates.

Dual Channel Mask Latches

The Dual Channel Mask Gates allow the user to block Image 1 and Image 2 bus bits on a bit-by-bit basis via a 16-bit mask word. The PS/2 writes the mask word to the memory mapped Dual Channel Mask Latches. The latches consist of two octal D-type latches located at X23Y160 (Image 1 mask bits) and X20Y160 (Image 2 mask bits). They are shown on sheet 27 of the schematics. DCM0-DCM7 (Dual Channel Mask 0-7) are mask bits for V10-V17 (latched Image 1 bits), respectively. DCM8-DCMF are mask bits for V20-V27 (latched Image 2 bits), respectively.

Dual Channel Mask Gates

The Dual Channel Mask Gates allow the user to block Image 1 and Image 2 video data on a bit-by-bit basis. The gates are controlled by outputs of the Dual Channel Mask Latches (described above).

The Dual Channel Mask Gates consist of 16, 3-input AND gates which are shown on sheet 27 of the schematics. The 3-input AND gates are used for Image 1 and Image 2 data bit masking. Each gate passes its respective data bit if its mask bit and VB1 (Video Blanking for Image 1 input gates) or VB2 (Video Blanking for Image 2 input gates) are high. The VB1 and VB2 inputs to the Dual Channel Mask Gates allow the user to turn off entire image channels. The Dual Channel Mask Latches inputs allow the user to turn off any input data bit or bits.

Masked Dual Channel Latches

The Dual Channel Mask Gates drive the Masked Dual Channel Latch. The latch consists of two cascaded D-type latches located at X23Y114 (latches the masked Image 1 video bits) and X20Y114 (latches the masked Image 2 bits). These tri-state latches resynchronize the data to the rising edge of PXLCK-K. They also function as part of a multiplexer consisting of the Dual Channel Palette Load Address Buffers and the Masked Dual Channel Latches. The Masked Dual Channel Latches are enabled during the visible scan lines by DVG/. The 16 output bits drive the 16 address inputs of the Dual Channel Palette RAM.

Dual Channel Palette Load Address Buffers

The Dual Channel Palette Load Address Buffers allow the PS/2 to address the Dual Channel Palette RAM during vertical blanking. Together with the Masked Dual Channel Latches, they also form an address multiplexer for the Dual Channel Palette RAM.
The Dual Channel Palette Load Address Buffers consist of two octal line drivers located at X23Y125 (eight LSBs) and X20Y125; they are shown on sheet 27 of the schematics.

The Dual Channel Palette RAM consists of 24 dual ported 64K by 1-bit static RAMs that are wired to function as a 64K by 24-bit RAM. These RAMs are shown on sheets 28-30 of the schematics.

Because the RAMs are dual ported, their D-inputs are driven directly by the FD bus. All 24 bits on the FD bus are written into the RAMs when WEDC/(Write Enable Dual Channel) goes low. This signal is an output of the Memory Mapped Control logic.

The 24 output bits of the Dual Channel Palette RAM are divided into eight bits each of red, green and blue. The RAMs on sheet 28 drive the Dual Channel Red bus (DCR0-DCR7); the RAMs shown on sheet 29 drive the Dual Channel Green bus (DCG0-DCG7); the RAMs shown on sheet 30 drive the Dual Channel Blue bus (DCB0-DCB7). During programming, FD00-FD07 provide red bus lookup data; FD08-FD0F provide green bus lookup data; FD10-FD17 provide blue bus lookup data.

The RGB outputs of the Graphics Channel, Image Channels 1 and 2, and the Dual Channel drive the Dual Channel Multiplexer.

The Dual Channel Multiplexer consists of four sets of tri-state D-type octal latches, one set for each data source. Each set consists of three latches. The Image 1 latch set consists of X37Y160, X35Y160 and X37Y125. The Image 2 latch set consists of X37Y149, X35Y149 and X37Y114. The Graphics latch set consists of X37Y136, X35Y136 and X35Y123. These latches are shown on sheet 32 of the schematics. The Red, Green and Blue Dual Channel latches are X17Y64, X14Y64 and X12Y64, respectively. They are shown on schematic sheets 28, 29 and 30, respectively.

Each latch set making up the Dual Channel Multiplexer resynchronizes its respective data input by latching its data on the rising edge of the pixel clock. The tri-state control for each latch set is driven by the Prioritizer. In addition, the latch sets driven by the Graphics Channel contain a Clear input (CLR - pin 1). Refer to the Prioritizer description (starting on page 5-64) for information on all multiplexer control signals.

The Dual Channel DAC is identical to the Channel 1 and Channel 2 DACs. Refer to the Channel 1 DAC description on page 5-77 for more information.
Timing Diagram 11. Alternate Line Gate Timing
Interlaced Dual Channel

The Interlaced Dual Channel logic is shown on sheet 33 of the schematics. The circuitry for each block in the Interlaced Dual Channel section shown on sheet 2 of Figure 6 (page 4-14) is described separately below.

Alternate Line Gate

The Alternate Line Gate consists of the NAND gate located at X35Y106B. It is driven by PXLCK-Q, BLANK/ (Composite Blanking) and OEL (Odd/Even Line). BLANK/ is applied to the gate via the D5/Q5 section of the D-type latch located at X41Y112 which resynchronizes BLANK/ with the pixel clock.

The blanking input to the NAND gate qualifies the gate's pin 4 input during the 640 visible pixels of every visible scan line. OEL qualifies the gate's pin 3 input every other visible scan line. Therefore, pixel clocks are gated through X35Y106B during the visible pixel portion of every other scan line. Timing Diagram 11 on the adjacent page shows the input and output waveforms of the Alternate Line Gate.

Pixel Clock Divide-By-Two

The Pixel Clock Divide-By-Two logic consists of NAND gates X35Y106A and X37Y106B, and latch X41Y112. X37Y106B and the D4/Q4 section of the latch divide the pixel clock frequency in half for use as a DAC clock drive. X35Y106A and the D3/Q3 section of the latch divide the pixel clock frequency in half for use as a FIFO read strobe.

X35Y106A generates read strobes for the Interlace FIFO. FIFO read strobes are required only during the visible pixel portion of the interlaced scan; they are one-half the frequency of the pixel clock. Read strobe generation is restricted to the interlaced visible pixel period by gating X35Y106A with NCB (NTSC Composite Blanking). When enabled by NCB, X35Y106A and the D3/Q3 section of X41Y112 function as a toggle flip-flop that changes state on the rising edge of PXLCK-F. Thus, the X35Y106A output frequency is PXLCK-F/2. The Empty Flag output of X43Y114 (pin 21) prevents X35Y106 from generating read strobes if the FIFOs are empty. X35Y106A's output drives the read pins (pin 15) on the FIFOs as well as a synchronizing input to X37Y106B.

X37Y106B and the D4/Q4 section of X41Y112 function as a toggle flip-flop that is enabled by the FIFO read strobe generator's output. If the phase relationship between the outputs of X35Y106A and X37Y106B are incorrect, X37Y106B is forced to wait an additional 0.5 interlaced clock periods before changing states. This causes the output of X37Y106B to resynchronize to the FIFO read strobe generator output. The Pixel Clock Divide-By-Two timing is shown in Timing Diagram 12 on page 5-82.
Timing Diagram 12. Pixel Clock Divide-By-Two Timing
Interlace FIFO

The Interlace FIFO consists of three cascaded 8-bit by 512-word FIFOs. The FIFO located at X47Y114 provides red data storage; the FIFO at X45Y114 provides green data storage; the FIFO at X43Y114 provides blue data storage. Refer to the Alternate Line Gate description on page 5-81 for FIFO data writing and timing information. Refer to the Pixel Clock Divide-By-Two description on that same page for FIFO data reading and timing information.

Interlaced Dual Channel DAC

The Interlaced Dual Channel DAC is located at X56Y129 and is shown on sheet 33 of the schematics. This DAC is identical to the Channel 1 and 2 DACs except for the input clock frequency and the NCS and NCB waveforms.

Interlaced Sync Driver

The Interlaced Sync Driver is located at X51Y120B and is shown on sheet 33 of the schematics. It is identical to the Channel 1 Sync Driver. Refer to page 5-77 for more information.
WIDE WORD Interlace Adapter Board
(Optional)

Some MciDAS users whose systems contain WIDE WORD Workstations have requested the ability to drive NTSC monitors with the Image Channel 1 and Image Channel 2 outputs. This may be especially desirable for those users who frequently configure the WIDE WORD Workstation for briefing frames.

The WIDE WORD Interlace Adapter Board converts the normally non-interlaced Image Channel 1 and Image Channel 2 outputs to interlaced format. It also converts the sync outputs for these channels to NTSC sync.

Functional Description

Refer to Figure 19 on page 5-87. The left side of this figure shows the output section of the A Board without the WIDE WORD Interlace Adapter Board (hereafter referred to as the adapter board) installed. It is identical to the output portion of the A Board Detailed Functional Block Diagram shown in Figure 6. The right side of Figure 19 shows the A Board output section when the adapter board is installed.

The WIDE WORD Interlace Adapter Board intercepts the Image Channel 1 and Image Channel 2 RGB drive inputs to the Channel 1 and Channel 2 DACs and converts these signals to interlaced formats. Functionally, the conversion process is identical to the Interlaced Dual Channel process. Refer to the Interlaced Dual Channel Description on pages 4-70 and 4-71 for a functional description of the Channel 1 and Channel 2 converters. Note that the Alternate Line Gate and Pixel Clock Divide-By-two blocks are not duplicated for the Channel 1 and Channel 2 converters. The outputs of these blocks in the Interlaced Dual Channel converter are shared by all three interlace converters.
Detailed Circuit Description

The adapter board is a 4.75 inch by 5.70 inch double sided printed circuit board that is mounted onto the A Board. When the A Board is placed on a horizontal surface, component side up and the top of the board pointing away from you, the adapter board is mounted on the far left corner of the A Board. Refer to the WIDE WORD Interface Adapter Installation Package instructions to properly install the adapter board.

SSEC's drawing number 6450-0633 is the schematic diagram for the WIDE WORD Interface Adapter Board. This schematic is located at the back of Appendix A. Also, refer to sheets 31 and 33 of the A Board schematics (6450-0563) as necessary. Since the Channel 1 and Channel 2 converters are identical, only the Channel 1 converter is described.

Refer to sheet 33 of the A Board schematics. The following control signals are either available to or generated by the Interlaced Dual Channel and are required by the adapter board:

- DVG (Delayed Vertical Gate)
- FIFO Write Strobes (output of NAND gate X35Y106B)
- FIFO Read Strobes (output of AND gate X35Y106A)
- NCS (NTSC Composite Sync)
- NCB (NTSC Composite Blanking)

The first three signals in the preceding list are available at the pins of the resistor pack located at X41Y123 (see sheet 33 of the A Board schematics). The last two control signals are available at pins 36 and 37 of the Interlaced Dual Channel DAC (X56Y129 on sheet 33 of the A Board schematics). Thus, by using the IC sockets at X41Y123 and X56Y129 as connector sockets between the A Board and the adapter board and relocating the resistor pack and DAC onto the adapter board, all required control signals are available to the adapter board.

Data signals required by the adapter board are the RGB non-interlaced DAC inputs for Channel 1 and Channel 2. By removing the Channel 1 and Channel 2 DACs located at X48Y150 and X56Y150, respectively, and using their IC sockets as connectors, these signals are available to the adapter board. The Channel DACs are relocated to the adapter board (U5 and U1).
The Channel 1 and Channel 2 Sync Driver IC is the remaining socket that is used as a connector between the two boards. Interlaced sync must replace the non-interlace sync for Image Channel 1 and Image Channel 2 when the adapter board is installed. Interlaced sync is substituted for the non-interlaced sync by relocating the sync driver chip to the adapter board and driving its inputs with the NCS signal (refer to sheet 31 of the A Board schematics and the schematic of the adapter board).

FIFO Read and Write Strobes

The Alternate Line Gate and Pixel Clock Divide-By-Two circuits generate FIFO write and read strobes, respectively. For information on these signals, refer the Interlaced Dual Channel description beginning on page 5-81.

Interlaced Image Channel 1 FIFO

The Interlaced Image Channel 1 FIFO consists of three parallel connected 8-bit by 512-word FIFOs. The FIFO located at U8 provides red data storage; the FIFO located at U10 provides green data storage; the FIFO located at U11 provides blue data storage. Refer to the Interlaced Dual Channel description for FIFO read and write timing information.

Channel 1 DAC

The Channel 1 DAC is located at U5. This DAC is identical to the Channel 1 DAC described on page 5-77 except for the input clock frequency and the NCS and NCB waveforms.

Channel 1 Sync Driver

The Channel 1 Sync Driver is located at U3. It is identical to the Channel 1 Sync Driver described on page 5-77.
A Board Output Section Without the WIDE WORD Interlace Adapter Board Installed

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A Board Output Section With the WIDE WORD Interlace Adapter Board Installed

Figure 19. WIDE WORD Interlace Adapter Board Functional Block Diagram

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B Board Simplified Functional Description

Figure 20 on the next page is the WIDE WORD B Board Simplified Functional Block Diagram. It divides the B Board into three sections:

- the PS/2 to B Board Interface
- the B Board to A Board Interface
- the B Board to Dataram Memory Interface

PS/2 to B Board Interface

The PS/2 to B Board Interface section is common to the other two B Board sections. It terminates the B Board's end of the PS/2 to Dataram interconnecting cable that carries 17 address lines, 16 data lines and 9 handshake/control lines. It consists of line drivers, line receivers, line transceivers, and memory and I/O mapped control decoding.

B Board to A Board Interface

Banks of FIFOs assemble address and data words. They provide storage and can be loaded individually and unloaded simultaneously. The FIFOs used in the B Board to A Board Interface allow up to 8192, 18-bit addresses and 24-bit data words to be assembled and stored. As described in the A Board chapters, data must be written to the A Board during the vertical blanking time. To maximize the data transfer during this time, addresses and data are assembled during the vertical scan time and enabled to the A Board during the vertical blanking time. Thus, up to 4096 addresses and their associated data words can be queued for transfer during the next vertical blanking period.
Figure 20. B Board Simplified Functional Block Diagram
B Board to Dataram Memory Interface

The B Board to Dataram Memory Interface consists of mode controls, a 32-bit address bus and a 128-bit bidirectional data bus. FIFOs assemble the address and data words.

Unlike the A Board data transfers that occur only during vertical blanking, Dataram memory transfers to and from the B Board are allowed during each horizontal scan time as soon as the A Board finishes reading the next line’s scan data. Dataram memory transfers are also allowed between horizontal sync times during the vertical blanking period. Thus, the Data and Address FIFOs do not need as much storage capacity as their B Board to A Board Interface counterparts (512 words versus 4096).

Read/Write Control

The Dataram Mode Controls consist of the Read/Write (R/W) Control block in Figure 20. The B Board to Dataram Memory Interface allows the following Dataram memory transfers:

- WIDE WORD Write (128-bit write, Mode 0)
- WIDE WORD Read (128-bit read, Mode 1)
- Read-Modify-Write Byte (byte write, Mode 2)
- Read-Modify-Write WIDE WORD (128-bit erase, Mode 3)

The transfer mode is defined by a 2-bit word from the PS/2. The WIDE WORD Write mode (Mode 0) loads image frames into memory. Sixteen consecutive pixels (one WIDE WORD) are stored at a time.

The WIDE WORD Read mode (Mode 1) allows the PS/2 to read a graphics or image frame previously stored in the Dataram memory, one 64K byte block at a time. Then the PS/2 can modify the frame and send it back to the Dataram memory via Mode 0.

The Read-Modify-Write Byte mode (Mode 2) consists of:

- a read phase
- a modify phase
- a write phase

During the read phase, a selected byte (i.e., one pixel of the display) within the addressed WIDE WORD is presented to the B Board. This byte is modified by the user via a bit mask and a modify data byte. The mask selects which bits within the byte are to be modified; the data byte determines if the selected bits are to be set or reset. During the write phase, the modified byte replaces the original byte in the WIDE WORD. Then the entire WIDE WORD is written back into memory at its original address.
The Read-Modify-Write WIDE WORD mode (Mode 3) erases one or more bit planes in a graphics frame. This mode is similar to Mode 2. However, instead of reading and modifying a single byte, the entire WIDE WORD is available. Also, each mask bit (8 mask bits total) is simultaneously applied to the corresponding bit of each byte within the WIDE WORD. Likewise, the corresponding bit of the modification byte is written to the corresponding bit of each WIDE WORD byte, providing the respective mask bit is high. Thus, from one to eight bits can be modified in each WIDE WORD byte simultaneously.

The Read/Write Control consists of a Dataram Mode Controller and a Dataram Interface Controller. The Dataram Mode Controller consists of handshake control signal logic and Dataram mode select logic. All Dataram memory transfers are controlled by these four interlocked handshake signals:

- Address Available
- Address Acknowledge
- Data Request
- Data Acknowledge

For memory reads or writes, the Read/Write Control logic enables an address to the memory and asserts Address Available. After the memory latches the address, it returns an Address Acknowledge, clearing the Address Available signal. Upon receipt of the Address Acknowledge, the Read/Write Control logic asserts Data Request which clears the memory's Address Acknowledge signal and initiates a memory read or memory write cycle. After the memory has either fetched or stored the requested data (read or write, respectively), the memory returns a Data Acknowledge, completing the cycle.

The Dataram Mode Select lines determine which of the four modes (Mode 0, 1, 2 or 3) will be executed. When Mode 2 is selected, the Dataram Control Interface also provides byte select lines.

The Dataram Interface Controller:

- provides clock and load strobes for the Address GeneratorLatch
- loads and unloads the Address and Data FIFOs
- provides read/write strobes for the Bus Flippers
- controls the Readback RAM

The operation of each of these blocks is modified by the mode code.
Address FIFOs

The Address FIFOs assemble 32-bit WIDE WORD addresses and present them to the Address Generator/Latch. The B Board memory modes are identified by a 2-bit mode code which is latched into a memory mapped latch within the Address FIFO block. When an address is stored in the Address FIFO, the contents of the mode latch (mode code) are also stored in the Address FIFO. Thus, this block stores a mode code for each address. This allows addresses and their respective modes to be queued up, eliminating the possibility of an address becoming disassociated from its intended mode. The user must ensure that the current contents of the mode latch are updated each time the memory mode is changed.

Address Generator/Latch

All memory read/write modes (Modes 0-3) used by the B Board require an address for each WIDE WORD or byte of a WIDE WORD. This is in contrast to the Sequential Read mode used by the A Board which requires only the starting address of a sequential block of WIDE WORDs.

Some B Board read/write operations are sequential in nature. For example, to read back an image or graphics frame or erase an entire graph, each WIDE WORD within the respective frame must be addressed. This makes automatic sequential addressing very desirable. However, when modifying a graph, the pixel currently being modified may not be adjacent to the next pixel needing modification. The Address Generator/Latch maximizes data throughput and reduces PS/2 addressing overhead. It functions as a latch in Modes 0 and 2; it functions as an up- or down-counter (selected via the PS/2) in modes 1 and 3.

Data FIFO

In Mode 0, the Data FIFO assembles 128-bit data words for storage in the Dataram memory. For Mode 1, the Data FIFO is loaded with Address Generator parameters (consisting of 20 bits) which define the line length and number of lines to be read. The remaining 108 data bits are not used in Mode 1. In Mode 2, the Data FIFO contains a 16-bit word that consists of the mask byte and the modification data byte. The remaining 112 bits are unused. In Mode 3, the Data FIFO contains parameters that are equivalent to those for Modes 1 and 2 combined. These parameters describe how many WIDE WORDs are to be modified and which bits in each byte are to be set or reset.
Bus Flippers and Readback RAM

The Bus Flippers consist of 128 logic cells, one for each data bit. Each cell consists of a latch and mask gates. When writing WIDE WORDs, the 128 data bits from the output of the Data FIFO pass through the Bus Flippers to the Dataram Data Bus. During WIDE WORD reading (Mode 1), Dataram data is latched internally in the Bus Flippers. The output of the latch drives the data input of the Readback RAM. It is also fed back to the mask gate inputs of the Bus Flippers.

During the Read-Modify-Write modes (Modes 2 and 3), the Data FIFO presents an 8-bit mask and an 8-bit data word to the Bus Flippers. During the read phase of the Read-Modify-Write cycle, the data is read from memory and latched into the internal latches of the Bus Flippers. This latched data is internally routed to the mask gates of the Bus Flippers where each bit is gated with its respective mask bit and modification data bit. If the respective mask bit is high, the old data bit is replaced with the new data bit; if the mask bit is low, the latched old data bit is retained. Finally, during the write phase of the cycle, the modified data word is written back into memory.

The Readback RAM consists of 16 cascaded byte-wide RAMs. The entire 128-bit data word is written to the Readback RAM in one write operation. Up to 4K words (64K bytes) may be stored in the Readback RAM. Data from the Readback RAM is passed to the PS/2 in 16-bit data words. Thus, one function of the Readback RAM is data word disassembly.
B Board Detailed Functional Description

Figure 21 on page 6-9 is the WIDE WORD B Board Detailed Functional Block Diagram. Each block in Figure 21 contains a sheet reference. These numbers show the schematic sheet numbers that apply to the particular block.

Figure 21 is supplemented with detailed block diagrams as necessary. Each block contains a location code that locates the IC chip that implements the function. The code consists of two numbers separated by an alpha character. The left number identifies the schematic sheet number; the alpha character and the right number are the vertical and horizontal grid coordinates, respectively, that describe the location of the chips on the schematic.
PS/2 to B Board Interface

The PS/2 to B Board Interface consists of the PS/2 Bus Interface and the Memory and I/O Mapped Control Decoder. See Figure 21.

PS/2 Bus Interface

The PS/2 Bus Interface consists of:
- a Data Bus Interface
- an Address Bus Interface
- a Control Interface

Data Bus Interface

The Data Bus Interface terminates the sixteen data lines with two noninverting octal transceivers. The B Board side of these transceivers connects to the B Board's Data Bus (DAT0-DATF). The PS/2 side of these transceivers connects to the PS/2-to-Dataram data bus (PCD0-PCD15).

Address Bus Interface

The Address Bus Interface terminates the seventeen PS/2-to-Dataram address bus lines (PCA0-PCA16) using line receivers. The output of these receivers drives the B Board's Address Bus (ADR0-ADR10).

Control Interface

The Control Interface consists of seven incoming lines from the PS/2 and one outgoing line to the PS/2. Four of the incoming lines identify PS/2 bus activity as one of the following:
- Memory Read
- Memory Write
- I/O Read
- I/O Write

One of the three remaining control lines drives the direction control on the bidirectional data bus transceivers. Another allows the PS/2 to initialize the workstation during power-up. The last control line identifies the active portion of the PS/2-to-Dataram's data bus. This bus can function as an 8- or 16-bit bus. In the 16-bit mode, this control line is asserted by the PS/2 when the data on PCD8-PCD15 is valid and stable. The control line driven by the B Board is a frame interrupt signal. This interrupt occurs at the NTSC vertical frame rate (approximately 30 interrupts/second). Upon interrupt, the PS/2 sends commands and data to the B Board to be used during the next frame.
Memory and I/O Mapped Control Decoder

The Memory and I/O Mapped Control Decoder asserts a specific control signal when an address from the PS/2 falls within a specified block of memory or I/O space. Each of its memory or I/O mapped control signal outputs is described below.

LDF0-LDFE

LDF0-LDFE (Load FIFO 0-E, respectively) are memory mapped FIFO load strobes that store the lower 15 bytes of each 16-byte WIDE WORD.

Most memory mapped devices on the B Board consist of FIFOs. Some of them assemble data words from the PS/2's 16-bit data bus into various sized data words required by the A Board and Dataram memory. For example, A Board color enhancement table loading requires 24-bit data words. The PS/2 begins by writing all the red data, followed by the green data and finally the blue data. This data is written directly into FIFOs whose load strobes are memory mapped. A similar process is performed when writing to the WIDE WORD memory where 16 bytes must be assembled for each WIDE WORD written into memory. Eight Micro Channel write cycles are required to assemble each 16-byte WIDE WORD. During each cycle, two 8-bit FIFOs must be strobed to store the 16-bit data bus word.

FAL

FAL (FIFO Address Load) is a dual purpose, memory mapped strobe. It strobes the lower 16 bits of the WIDE WORD address into the Address FIFO. This forms the 16 LSBs of the address that the data is destined for in the WIDE WORD memory. It also strobes the most significant byte of the 16-byte WIDE WORD into the Data FIFO.

UBS

To modify or erase all or part of a graphics frame, the Read-Modify-Write Byte or Read-Modify-Write WIDE WORD Dataram mode, respectively, must be used. During these modes, the PS/2 transfers the modify data byte and the modify mask byte as two single byte transfers, one byte per write cycle. The modify data byte is written to address 10000H; the mask is written to address 10001H. Note that the address LSB is low during the first transfer (data) and high during the second transfer (mask). Therefore, the PS/2 transfers the data byte on the lower half of the data bus (PCD0-PCD7) followed by the mask on the upper half of the data bus (PCD8-PCD15). ADR0 (address LSB) and BHEN (Byte High Enable) determine which half of the data bus is currently active. During the Read-Modify-Write modes, ADR0 forms UBS (Upper Byte Select). UBS controls a bus selector that selects the active half of the data bus as the data source when loading the respective FIFO in the Data FIFO block for a Read-Modify-Write cycle.
**ALC**

ALC (Address Latch Clock) is required for LDF0-LDFE or FAL to be asserted. ALC is asserted when the PS/2 writes to an address from 10000H-1FFFFF.H. This block of memory mapped address space is reserved for Dataram memory reading/writing.

**RR0/-RR1/**

RR0/ and RR1/ (Raster Read 0-1, respectively) are read byte enables when the PS/2 reads data from the WIDE WORD memory. The PS/2 must read the 16-byte WIDE WORD one or two bytes at a time. ADR1-ADR3 select a two-byte component of the addressed WIDE WORD. Then, RR0/ and RR1/ select the byte or bytes from that group for transfer to the PS/2. The PS/2 can read the high byte only, the low byte only or both bytes simultaneously via its BHEN (Byte High Enable) and PCA0 (address LSB) signals. Table 25 below summarizes the data transfer possibilities when the PS/2 reads the Dataram memory.

<table>
<thead>
<tr>
<th>BHEN/*</th>
<th>A0</th>
<th>RR1/*</th>
<th>RR0/*</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Low byte only</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>High byte only</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Both bytes</td>
</tr>
</tbody>
</table>

* Active low signals

**Table 25. Readback Control**

**UAW**

The PS/2 Bus Interface contains 17 address lines. Since the MSB (ADR10) is used for data steering (1 or 0 selects Dataram or A Board, respectively), only 16 address lines are available for addressing. Passing data to or from the WIDE WORD requires a 32-bit address. The upper 16 address bits are specified by writing a 16-bit data word to a pair of octal D-type latches. These latches are clocked by UAW (Upper Address Write) when the PS/2 writes to I/O port 33EH. Thus, before writing to the WIDE WORD, the user must do a port 33EH write to set the upper 16 address bits. The 16 LSBs of the Address Bus (ADRO-ADRF) directly drive the 16 address LSBs. The user writes (or reads) data to (or from) any address within the 64K address block selected by the upper address word.
CMW

CMW (Change Mask/Mode Write) is asserted when the PS/2 writes to I/O port 33CH. CMW latches the 12 LSBs of the data bus when it is asserted. Latched DAT0-DAT7 is the Change Mask; DAT8-DATB is the mode word.

DAT0-B are latched in two D-type latches, an octal latch and a quad latch. The octal latch latches DAT0-DAT7 and forms the Mask Latch block in Figure 21. The quad latch latches DAT8-DATB and is called the Mode Latch in Figure 21. The LSB output of the Mode Latch (driven by DAT8) controls the Address Generator’s count direction and is not part of the Dataram transfer mode. The 2-bit Dataram transfer mode code consists of MC0 and MC1 which are driven by DAT9 and DATA, respectively. The latched output driven by DATB is not used. Table 26 below shows the mode code and the selected Dataram mode.

<table>
<thead>
<tr>
<th>MC1</th>
<th>MC0</th>
<th>Mode</th>
<th>Dataram Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>WIDE WORD Write</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>WIDE WORD Read</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2</td>
<td>R-M-W Byte</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>R-M-W WIDE WORD</td>
</tr>
</tbody>
</table>

Table 26. B Board Transfer Modes

Since data transfers between the PS/2 and the WIDE WORD memory occur only when the A Board is not reading from memory, PS/2 data destined for the WIDE WORD memory is queued in FIFOs. Since each transfer may have a different mode, the mode is stored with the data and address. This eliminates any possibility of the data, address and mode becoming disassociated.

STAT/

STAT/ (Status) is an I/O mapped enable input to the Status Port that is asserted when the PS/2 reads I/O port 33Eh. The Status Port allows the PS/2 to read the status of 28 FIFOs.

FIFOs do not respond to additional load strobes when they are full. The PS/2 can read the Status Port prior to writing to ensure that the destination FIFO will accept the new data (FIFO is not full). The FIFOs monitored by this port are the 16 WIDE WORD Data FIFOs, the 4 WIDE WORD Address FIFOs, the 6 A Board Data FIFOs, and the 2 A Board Address FIFOs.

STAT/ also provides a Mode 1 READ DONE status.
MSL (Memory Block Select Latch) is asserted when the PS/2 writes to I/O port 336H. MSL latches a D-type latch that establishes the two MSBs of the A Board's 18-bit address (UFA10-UFA11).
B Board to A Board Interface

The B Board to A Board Interface consists of a Data Bus Interface, an Address Bus Interface and an Interface Control. Refer to Figure 21 on page 6-9 as necessary.

Data Bus Interface

The Data Bus Interface, which consists of the A Board Data FIFO block in Figure 21, is made up of six 4K by 8 FIFOs. Each FIFO has its own memory mapped load strobe. FIFOs are loaded individually or in groups of two. They are functionally organized as two 24-bit banks during unloading. A Board data destinations require 1-, 2- or 3-byte word lengths. The A Board Data FIFO assembles the proper length words for the data destinations on the A Board.

Address Bus Interface

The Address Bus Interface, which consists of the A Board Address FIFO and the A Board Upper Address Port blocks, uses ADR10 to determine if an address from the PS/2 is part of an A Board address or a Dataram address. If ADR10 is low, the ADR0-ADRF address is intended for the A Board; if ADR10 is high, it is intended for the Dataram. ADR10 must be low to enable the A Board FIFO Load Strobe Generator block.

ADRO-ADRF directly drive the 16 LSB data inputs of the A Board Address FIFO. The drives for the two MSBs of the address are supplied to the A Board Address FIFO by the A Board Upper Address Port. This port, consisting of a D-type latch, latches the 4 LSBs of the Data Bus (DAT0-DAT3) when MSL is asserted. This signal is asserted when the PS/2 writes to I/O port 336H. The 18 address bits are loaded into the A Board Address FIFO by a load strobe from the A Board FIFO Load Strobe Generator. The A Board Address FIFO functions as a 4K by 18-bit address queue.
Control Interface

The Control Interface consists of the A Board FIFO Load Strobe Generator block in Figure 21. This block generates the FIFO load and unload strobes for the A Board Address and Data FIFO blocks.

The A Board Data FIFO consists of six 4K by 8 FIFOs. These FIFOs can be loaded singly or in groups of two from the Data Bus (DAT0-DATF). During unloading, they are configured as an upper bank and a lower bank of three FIFOs each. Each bank’s tri-state outputs are multiplexed onto the UFD00-UFD17 data bus by its respective read strobe, i.e., LFR or UFR (Lower FIFO Read or Upper FIFO Read, respectively). These FIFO read strobes are generated by the Control Interface.

Each of the six A Board Data FIFOs is loaded by asserting its respective load strobe (FL0-FL5). FL0, FL2 and FL4 are lower bank load strobes; FL1, FL3 and FL5 are upper bank load strobes. The load strobe generated for a transfer is a function of address (A Board destination) and data bus word size (one or two bytes).

The Control Interface block generates one additional load strobe (FL6) that loads ADR1-ADRF and a 2-bit output of the A Board Upper Address Port into the A Board Address FIFO. Note that ADR0 (address LSB) is not FIFOed. UFA00, the address LSB output to the A Board, is generated during the FIFO read cycles.

During a typical transfer, the lower FIFO bank is enabled to the A Board with the output of the A Board Address FIFO and UFA00. At this time, UFA00 is low. Then, while the A Board Address FIFO is still enabled (drive UFA01-UFA11), the upper FIFO bank and UFA00 are enabled to the A Board. During this time, UFA00 is high. UFA00-UFA11 are latched twice on the A Board during a B Board to A Board transfer, once while the lower FIFO bank is enabled (UFA00 is low) and once while the upper bank is enabled (UFA00 is high).
B Board to Dataram Memory Interface

The B Board to Dataram Memory Interface transfers data between the PS/2 (via the PS/2 Interface) and the Dataram memory. These transfers are executed in one of the following modes:

- WIDE WORD Write (Mode 0)
- WIDE WORD Read (Mode 1)
- Read-Modify-Write Byte ((Mode 2)
- Read-Modify-Write WIDE WORD (Mode 3)

Mode 0 loads image and graphics frames into the Dataram memory.

Mode 1 allows the PS/2 to read back an image or graphics frame. After the PS/2 reads a frame, it can modify that frame and send it back to the Dataram memory via Mode 0.

Mode 2 is used for single pixel writing (writing graphics). In this mode, the Dataram executes two interlocked cycles, a read cycle and a write cycle. During the read cycle, the Dataram memory internally reads an entire WIDE WORD, but sends only the byte selected by the byte select lines to the B Board. Any or all bits within the selected byte can be modified by the B Board and returned to the Dataram memory during the write cycle. When the memory receives the modified byte, it replaces the originally selected byte with the modified byte and rewrites the entire WIDE WORD to its original address. Mode 2 can also modify a single point within a single bit plane, i.e., change 1 bit in one byte of a graphics frame.

Mode 3 erases bit planes; it can also be used with graphics frames. Up to seven graphs can be stored in each graphics frame by assigning each graph to a specific bit (bit plane) within each byte. For example, bit 1 of each byte of each WIDE WORD within the graphics frame (bit plane 1) could show U.S. state boundaries; bit 2 could show pressure contours; bit 3 could show temperature contours; etc. If a user wanted to erase the pressure contour, bit 2 of every byte within the addressed graphics frame must be set to zero. In Mode 3, the PS/2 sends a mask byte and a modification byte to the B Board. Each bit of the modification byte is directed to a corresponding bit within each byte of a currently addressed WIDE WORD. The modification bit replaces the original bit if its corresponding mask bit is high. If a mask bit is low, the corresponding data bit is unchanged.
In this example, only mask bit 2 (bit plane 2 mask bit) is set, allowing only modification bit 2 to be recognized. This bit must be set to zero to erase bit plane 2 bits. After modifying each byte of each WIDE WORD in the entire graphics frame, the pressure contour will disappear, but the U.S. state boundaries and temperature contour graphs will remain (as well as any graphs residing in bit planes 4-7). Since there is a separate mask and modification bit for each bit plane, any combination of graphs can be erased simultaneously.

Hardware configuration of the B Board to Dataram memory is influenced by the transfer mode code. Therefore, where appropriate, functional descriptions of the blocks in Figure 21 that are part of the B Board to Dataram Memory Interface are provided for each mode.
Read/Write Control

The Read/Write Control block shown in Figure 20 consists of the following blocks in Figure 21:

- Dataram Control and Byte Select
- Address Generator Controller
- Subcycle Repeat Counter
- Cycle Control Logic
- Memory Size Buffer
- FIFO Status Port

Dataram Control and Byte Select

The Dataram Control and Byte Select block drives the Dataram mode control input lines and interacts with the Dataram's four handshake signals.

The Dataram memory can operate in 84 modes, but the B Board only uses four of them:

- WIDE WORD Write (128-bit write, Mode 0)
- WIDE WORD Read (128-bit read, Mode 1)
- Read/Modify/Write Byte (byte write, Mode 2)
- Read/Modify/Write WIDE WORD (128-bit erase, Mode 3)

These modes are selected by mode control lines to the memory. Three mode selection and eight byte selection signals determine the mode. These signals are:

- WENSQ/ (WIDE WORD Enable Sequential)
- WREAD/ (WIDE WORD Read)
- WWBW1/ (WIDE WORD Bus Word)
- WWB00-WWB07/ (WIDE WORD Byte Select Lines)

WENSQ/ is low only during sequential reading or writing. This signal is driven by the A Board only. When the A Board controls the memory, WENSQ/ is low; when the B Board controls the memory, WENSQ/ is high.
WREAD/ is low during memory read cycles. Thus, it is driven low by the B Board during Mode 1 (WIDE WORD Readback) and during all Read/Modify/Write modes. Although the Read/Modify/Write modes contain a read and a write cycle, WREAD/ is defined as a low signal for both the read and write cycles. WREAD/ originates in the Cycle Control Logic block and is passed to the Dataram Control and Byte Select block as WRD (WIDE WORD Read).

WWBW1/ selects the upper or lower 64-bit data bus during byte operations. That is, it must be used with the WIDE WORD Select lines (WWB00/-WWB07/) to determine which bytes are being read from or written to memory. Except during WIDE WORD operations (Modes 0 and 1), the lower data bus (bits 0-63) is selected when WWBW1/ is high and the upper data bus (bits 64-127) is selected when WWBW1/ is low.

WWB00/-WWB07/ select the bytes to be read from or written to memory during Mode 2 (Read/Modify/Write Byte). The eight select lines correspond to the eight bytes of the data bus selected by WWBW1/. If all lines are concurrently high and WENSG/ is high, a nonsequential WIDE WORD (128 bits) cycle is specified. During this time, WREAD/ determines whether the cycle is a WIDE WORD write (Mode 0) or read (Mode 1).

Handshake Control deals with these four interlocked handshake signals:

- WADAV/ (WIDE WORD Address Available)
- WADAC/ (WIDE WORD Address Acknowledge)
- WDTRQ/ (WIDE WORD Data Request)
- WDTAC/ (WIDE WORD Data Acknowledge)

For functional information on these signals, see page 6-4.
Address Generator Controller

The Address Generator Controller controls the WIDE WORD Address Generator/Latch and provides an input to the Subcycle Repeat Counter.

The Address Generator/Latch is either in a load or count mode. Mode control is accomplished by the Load signal. If Load is low, the Address Generator/Latch is preset to the current output of the Write Address/Mode FIFO; if Load is high, the Address Generator/Latch increments or decrements. The generator's latch's clock is driven by the Clock output of the Address Generator Controller which uses the FIFOed Mode signals to determine if the Address Generator/Latch should be loaded and/or clocked.

The Address Generator Controller also provides a Load and Clock input to the Subcycle Repeat Counter. These signals are a function of mode and are respectively in phase with the Load and Clock inputs to the Address Generator/Latch.

Subcycle Repeat Counter

The Subcycle Repeat Counter is used in Modes 1 and 3 only. It determines how many consecutive addresses can be accessed.

Prior to beginning a Mode 1 or 3 cycle, the Subcycle Repeat Counter is preloaded with the number of WIDE WORDs to be read or written. Each time a word is transferred to or from memory, the counter is decremented. Upon reaching zero, the counter generates a Cycle Stop signal.

In Modes 1 or 3, the Cycle Stop signal controls the generation of GO (by the Cycle Control Logic). Until Cycle Stop is asserted, a new GO signal is generated after the completion of each word transfer. The Address Generator Controller generates a clock pulse for the WIDE WORD Address Counter Latch and the Subcycle Repeat Counter on the rising edge of GO.

The Subcycle Repeat Counter has a line length section and a line counter section. The product of the count loaded into these sections must equal the number of words to be transferred. The line length section has a range of 0-4095\textsubscript{10} (000-FFF\textsubscript{16}); the line counter section has a range of 0-255\textsubscript{10} (00-FF\textsubscript{16}). Thus, the Subcycle Repeat Counter has a product range of 0-1,048,575\textsubscript{10} words (0-FFFF\textsubscript{16}). A portion of the Write Data bus (D200-D390) carries the programming information for the Subcycle Repeat Counter. Refer to the Write Data FIFO section on page 6-29 for more information on the Write Data bus.
Cycle Control Logic

The Cycle Control Logic block is the heart of the B Board control. This block generates several control signals that are initiated by the rising edge of GO.

GO must be asserted for any B Board access of the Dataram memory. GO causes the WIDE WORD Address Generator Controller to send a valid address to the memory. It also causes the Dataram Control and Byte Select block to initiate WADAV/, the first of four interlocked handshake control signals. The last interlocked handshake signal (WDTAC/-WIDE WORD Data Acknowledge) clears GO. Because Modes 1 and 3 consist of multiple read or write cycles from or to sequential memory addresses, GO must be reasserted for each access.

GO is asserted if Raster Read Done is asserted and Memory Busy is false (not busy). Raster Read Done is a board access multiplexing signal that is asserted by the A Board when it is not doing a Raster Read or Refresh cycle. This tells the B Board that it can access the Dataram memory.

Upon initiation of a memory access cycle, the memory asserts Memory Busy. It clears this signal as soon as it can respond to a new access request. For Modes 1 and 3, GO is reasserted on the trailing edge of Memory Busy if additional access cycles are required.

Eighty nanoseconds before GO is first asserted, FR/ (FIFO Read) is asserted. This signal reads the next WIDE WORD address and mode from the Write Address/Mode FIFO. Although thousands of words may be read or erased (Mode 1 or 3, respectively) during a Readback or Erase command, FR/ is asserted the entire time from 80 nsec before the first read or write cycle to the completion of the last read or write cycle.

Modes 1 and 3, once initiated, continue until Cycle Stop is asserted by the Subcycle Repeat Counter. Prior to beginning one of these modes, the Subcycle Repeat Counter is preloaded with the required number of access cycles.

During Mode 1, the Mode 1 Done signal is asserted on the trailing edge of FR/. This signal is an input to the Status Port. After the PS/2 requests a Readback (Mode 1), it reads the Status Port to determine if the Readback cycle has finished. Upon finishing, the PS/2 will read the Readback RAM.

WRD and WTG (WIDE WORD Read and Write Gate, respectively) are read and write enable signals to the Bus Flippers. These signals are described in the Bus Flippers section on page 6-30.
Memory Size Buffer

The Address Over Range Protect Logic description on page 6-27 explains how an out-of-range address, is remapped to an in-range address, which prevents the memory from hanging up. However, this results in writing to an address that may be part of a graphics or image frame. The Address Over Range Protect Logic is a "fail safe" circuit. That is, it normally isn’t used.

The Dataram determines its memory size and outputs this information on its WSZ00/WSZ11/WIDE WORD Size) bus. The WSZ bus connects to the DATO-DATF bus via the Memory Size Buffer. This buffer is enabled by MSIZ (Memory Size), a memory mapped control signal from the Memory and I/O Mapped Control Decoder. This signal is asserted when reading I/O port 336H.

During McIDAS-OS2 setup, the PS/2 reads port 336H to determine the maximum in-range address of the Dataram memory. McIDAS-OS2 uses this information in frame allocation calculations. Thereafter, all Dataram accesses are automatically in range.

FIFO Status Port

The Status Port receives FIFO Full status from 24 B Board FIFOs. It also receives a Mode 1 Done signal from the Cycle Control Logic. It combines these signals into eight status signals and passes them to the DATO-DATF bus. The Status Port is enabled while reading I/O port 33E4H.
Address FIFOs

The Address FIFO block in Figure 20 on page 6-2 consists of the Write Address/Mode FIFO, WIDE WORD Upper Address Port Latch and the Mode Latch blocks in Figure 21.

Dataram memory access is multiplexed between the A and B Boards. A data throughput bottleneck would occur if the PS/2 attempted to write directly to the Dataram while it was busy with A Board activity. Further, the Dataram requires a 32-bit address. Since the WIDE WORD PS/2 Interface provides only 17 address lines (MSB is used as a destination flag only), the WIDE WORD address must be assembled. In addition, each WIDE WORD address requires a mode tag.

Write Address/Mode FIFO

The Write Address/Mode FIFO, consisting of four parallel cascaded 9-bit by 512-word FIFOs, functions as a 512 by 36-bit queue. Two bits provide mode storage; 32 bits provide Dataram address storage; one bit stores the Address Generator/Latch's count direction (up or down); one bit is unused.

The low order 16 address bit inputs to the FIFOs are provided by the 16 LSBs of the address bus (ADR0-F). The high order 16-bit input to the FIFOs is provided by the WIDE WORD Upper Address Port Latch. The 2-bit mode input is supplied by the Mode Latch.

The Write Address/Mode FIFO is loaded by writing to addresses 10000H-1FFFFFH. Writing to these addresses asserts FAL (see page 6-11). Read control of the Write Address/Mode FIFO is provided by the Cycle Enable Logic (READ). This block also provides a FIFO Full status to the Status Port. Prior to writing to the Write Address/Mode FIFO, the PS/2 reads the Status Port to determine if the Write Address/Mode FIFO is currently full. If the FIFO is full, the PS/2 continues to read the port until the Full condition clears, i.e., at least one address is unloaded from the FIFO by the Cycle Enable Logic.

WIDE WORD Upper Address Port Latch

The WIDE WORD Upper Address Port Latch provides the upper 16 bits of the WIDE WORD address to the Write Address/Mode Latch. DAT0-DATF drive the data inputs of the latch and UAW (Upper Address Write-I/O port 33EH Write) strobes this data into the latch. The output of this latch is a page address for the Dataram. It selects a 64K word block of Dataram memory to be addressed by ADR0-F. Thus, the latch needs to be written to only if the next Dataram address falls outside the current page's range.
Mode Latch

The Mode Latch is an I/O mapped 4-bit D-type latch which is strobed by CMW (Change Mask/Mode Write-I/O port 33CH Write). The D-inputs of this latch are driven by DAT8-DATB. The output bit, which is determined by the DAT8 input, controls the Address Generator/Latch’s count direction (increment or decrement). MC0 and MC1, the mode control signals, are driven by DAT9-A, respectively. Table 15 below defines the mode.

<table>
<thead>
<tr>
<th>MC1</th>
<th>MC0</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>(0) WIDE WORD Write (128 bits)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>(1) WIDE WORD Read (128 bits)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>(2) Read-Modify-Write Byte (8 bits)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(3) Read-Modify-Write WIDE WORD (128 bits)</td>
</tr>
</tbody>
</table>

Table 27. B Board Mode Codes
Figure 22. WIDE WORD Address Generator/Latch
Address Generator/Latch

The Address Generator/Latch can act as an address counter or an address latch. Its function is determined by the mode code that is stored with each address in the Write Address/Mode FIFO. Refer to Figure 21.

Regardless of mode, the Address Generator/Latch provides a 32-bit address to the WIDE WORD memory for every WIDE WORD read or write cycle. The Address Generator Controller determines whether the next WIDE WORD address is generated by incrementing (or decrementing) the count in the Address Generator/Latch (counter mode) or latching the output of the Write Address/Mode FIFO (latch mode).

Figure 22 on the adjacent page is an expansion of the WIDE WORD Address Generator/Latch block shown in Figure 21. The Generator/Latch consists of these three blocks:

- Address Counter and Latch
- Address Over Range Protect Logic
- Bus Drivers

Address Counter and Latch

The Address Counter and Latch consists of three 8-bit and one 4-bit cascaded, presettable, up/down counters. Together, these chips function as a presettable 28-bit up/down counter. The Load (ACL-Address Counter Load) input from the Address Generator Controller determines whether the Address Counter and Latch functions as a counter or a latch. If Load is high, the counter/latch counts up or down; if Load is low, the counter/latch latches (loads) the 28 LSB inputs from the Write Address/Mode FIFO. The 29th bit (MSB) is the direction control for the Address Counter and Latch (counter mode only).

Address Over Range Protect Logic

The Address Over Range Protect Logic prevents the PS/2 from writing to nonexistent memory. If the Dataram memory receives an address outside its physical range, the handshake logic fails and the memory must be reset (powered down) to recover. This is caused by the interlocked handshake between the B Board and the memory. When nonexistent memory is addressed, no Data Accepted signal is generated by the memory, preventing the current cycle from completing.
The Address Over Range Protect Logic compares the current address with the memory's size (WSZ00/WSZ11). If the address is in-range, this block enables the Bus Drivers' upper address output lines. If the address is out-of-range, the Bus Drivers' upper address output lines are tri-stated and the Bus Drivers block drives only the 20 LSBs of the address. Thus, reading from or writing to an out-of-range address results in remapping the out-of-range address to an address between 00000H and 0FFFFFH (0000 to 256K).

**Bus Drivers**

The Bus Drivers drive the 28 LSBs of the 32-bit Dataram address bus with the 28 address outputs of the Address Counter and Latch. The 4 MSB Bus Driver inputs are grounded. Thus, the resulting 4 MSB outputs are always logic zeros. These bits are used by Dataram to daisy chain multiple WIDE WORD chassis. Since all workstations use a single WIDE WORD chassis, these bits are always logic zeros.
Data FIFO

The Data FIFO section shown in Figure 20 consists of the Write Data FIFO block and the Modify Data and Mask Latch block in Figure 21.

Write Data FIFO

The Write Data FIFO block consists of 16 parallel cascaded 512 by 9-bit FIFOs and FIFO reset logic. Eight bits of each FIFO are used for data; the ninth bit is used for read error detection. The Write Data FIFO has a separate load strobe input for each FIFO (16 strobes total). The load strobe inputs are LDFO-LDFE (Load Data FIFOs 0-E, respectively) and FAL (FIFO Address Load). FAL loads the most significant byte into the Write Data FIFO; it strobes the least significant 16 address bits into the Write Address/Mode FIFO. The 16 FIFOs in the Write Data FIFO are read simultaneously by FR/ (FIFO Read). When writing to the Write Data FIFOs, all FIFOs must be written to, even if some of the individual FIFO's data bits aren't used, to prevent data skewing.

The data inputs of the Write Data FIFO are driven by the Data Bus (DAT0-DATF) and the BP Bus (BP0-BPF). The BP Bus drives the data inputs of the two least significant FIFOs; the Data Bus drives the data inputs of the 14 most significant FIFOs. For information on the BP Bus, see the Modify Data and Mask Latch description below.

Occasionally, a FIFO may "hang up" and remain in a tri-state condition when it is supposed to be enabled. This condition is detected by programming the ninth bit of each Write Data FIFO with a zero during FIFO loading. During Write Data FIFO reading, the ninth bit of each FIFO is checked for zero (low output). If a high level is detected on the ninth bit of any of the FIFOs in the Write Data FIFO block during FIFO reading, that FIFO is hung up and must be reset. The FIFO reset logic is an integral part of the Write Data FIFO block.

Modify Data and Mask Latch

The Modify Data and Mask Latch consists of an 8-bit multiplexer, an octal buffer and an octal latch. The multiplexer drives the BP0-BP7 outputs with DAT0-7 or DAT8-F. It allows a Data Bus byte from either the lower half (DAT0-DAT7) or upper half (DAT8-DATF) of the Data Bus to drive the lower eight bits of the BP Bus.

BP8-BPF are driven by the latch output or the buffer output as a function of the transfer mode. During Modes 0 and 1, the buffer drives BP8-BPF using DAT8-DATF, respectively; during Modes 2 and 3 (Read-Modify-Write modes), the latch drives BP8-BPF. The latch's inputs are driven by DAT0-DAT7. It is latched by CMW (Change Mask Write - I/O port 33CH Write). The latch outputs provide the mask word to the least significant FIFO during Modes 2 and 3.
Bus Flippers

The Bus Flippers block contains a 128-bit bidirectional data bus driver, latch and data director. Its function is determined by the current transfer mode (Modes 0-3). Refer to Figure 21. Each of the 128 output bits of the Write Data FIFO is applied to a logic cell consisting of:

- three AND gates
- one OR gate
- a tri-state buffer
- a D-type latch

Each logic cell is part of a PAL. Each PAL functions as a logic cell for four data bits. Thirty-two PALS, organized by bit plane nibbles, make up the Bus Flippers block. The data, control inputs and output pins for each PAL are shown in Figure 21. Note that some inputs and outputs show four pins. These pin numbers correspond to the four bits handled by the PAL.

WRD (Write Data) determines which AND gates are enabled; it is an output of the Cycle Control Logic block. WRD is low during Mode 0 and high during Modes 1-3. Therefore, the upper AND gate in Figure 21 is enabled in Mode 0; the lower two AND gates are enabled in Modes 1-3.

The upper AND gate of each logic cell passes a data bit to the tri-state buffer via the OR gate in Mode 0 (128 bits total). These bits are passed to the Dataram memory when the buffer is enabled by WTG (Write Gate).

The lower two AND gates are enabled by WRD during Modes 1-3. However, WTG, the buffer’s enable input, is valid only in Mode 0 and the write phase of the Read-Modify-Write modes (Modes 2-3). Therefore, the lower two AND gates, which pass write data to the Dataram memory, are functional only during Modes 2 and 3.

The Dataram output (read) data is applied to the D-input of each logic cell’s latch. The Read Clock strobes this data into the latch when the data is stable. The latch’s outputs drive the inputs of the Readback RAM and the lower AND gate. The lower AND gate input (old data) is gated to the tri-state buffer if the Mask input is low and the Mode is 2 or 3. If the Mask input is high, the middle AND gate is enabled in Modes 2 and 3, gating the Modification data to the tri-state buffer. During the write phase of the Read-Modify-Write cycle, the output of the middle or lower AND gate is gated to the Dataram memory by WTG.
Readback RAM

The Readback RAM section allows the PS/2 to read up to 64K bytes of a graphics or image frame. This section was introduced in Figure 20 and consists of the following blocks in Figure 21:

- Readback RAM
- Readback Address Multiplexer
- Word Selector

The B Board cannot respond immediately to a Readback request if the Dataram memory is being used by the A Board. If the B Board attempts a Dataram memory read or write cycle at this time, the PS/2 must wait until the A Board completes its use of the memory. This temporarily "hangs up" the PS/2, reducing its data throughput. This limitation is overcome by sending the B Board a set of fetch parameters which fetch and buffer the requested data. When the requested data is buffered on the B Board, the Mode 1 Done status flag informs the PS/2 that its requested data is ready. The PS/2 can then read the data from the buffer, uninterrupted by the A Board.

The fetch parameters consist of a line length and line count to the Subcycle Repeat Counter, and a mode (Mode 1) and start address to the Write Address/Mode FIFO. At the start of the Mode 1 cycle, the start address is downloaded to the WIDE WORD Address Generator/Latch. The lower 14 bits of the Dataram address are copied onto the BAT0-BATB bus which drives the Readback RAM's address inputs via the Readback Address Multiplexer. Thus, the WIDE WORD Address Generator/Latch addresses the Dataram memory and the Readback RAM at the same time.

Readback RAM

The Readback RAM can store up to 4096, 128-bit words, a capacity of 64K bytes. It consists of 16 parallel, cascaded, byte-wide static RAMs. The Readback RAM stores and reads 128-bit data words. The data output drives the input of the Data Selector.

Dataram output data (Readback data) is applied to the Bus Flippers, which latch this data and present it to the Readback RAM's data input.
**Readback Address Multiplexer**

The Readback Address Multiplexer drives the Readback RAM's address inputs. The PS/2, via the Address Bus (ADR0-ADR7), and the WIDE WORD Address GeneratorLatch provide inputs to the Readback Address Multiplexer. The multiplexer selects the WIDE WORD Address Generator/Latch to drive the RAM during the Dataram memory readout. It selects the PS/2 as the address source after the memory readout process completes.

**Word Selector**

The WIDE WORD Readback data stored in the Readback RAM must be transferred to the PS/2 over the 16-bit data bus. Therefore, the WIDE WORDs must be disassembled into bytes or double bytes (8-bit or 16-bit words, respectively). The Word Selector allows the PS/2 to read the data as if the Readback RAM was organized as a 64K byte or a 32K by 16-bit random access buffer. ADR1-ADR3 function as a double byte select address. Table 28 defines the address to data relationship.

<table>
<thead>
<tr>
<th>ADR3</th>
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<th>ADR1</th>
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<th>Readback RAM Bits</th>
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<td>0</td>
<td>0</td>
<td>0-1</td>
<td>0-15</td>
</tr>
<tr>
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<td>4-5</td>
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<td>6-7</td>
<td>48-63</td>
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<td>8-9</td>
<td>63-79</td>
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<tr>
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<td>1</td>
<td>0</td>
<td>12-13</td>
<td>96-111</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>14-15</td>
<td>112-127</td>
</tr>
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</table>

Table 28. Word Selector Addressing

RR0/-RR1/ (Readback RAM) are byte enables for the 16-bit word selected by ADR1-ADR3. RR0/, when low, enables the low order byte onto the Data Bus; RR1/, when low, enables the high order byte onto the Data Bus. Both bytes are enabled onto the Data Bus when both enables are low.
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<td>7-23</td>
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B Board Detailed Circuit Description

The schematic diagrams of the WIDE WORD B Board are shown on SSEC drawing 6450-0565 (Revision V3, dated 07/19/89). This Detailed Circuit Description discusses the logic of each block shown in the functional block diagram in Figure 21 on page 6-9. Refer to Figure 21 and the schematics as necessary.

Schematic Conventions

The WIDE WORD B Board is built on a Dataram multilayer form factor board. Locations on the board are described by the row designator (X1-X60) and column designator (Y1-Y169). Each schematic circuit symbol is labeled by the XY coordinate of its pin 1 location. The Detailed Circuit Description that follows refers to ICs by this location label. A reference to a schematic circuit symbol of a multiple section device uses the symbol ID followed by a letter designator. The symbol ID alone refers to single function ICs.

Logic Conventions

Logic signals are indicated by all uppercase letters and numbers, e.g., PSHL. A logic signal name ending with a trailing slash represents an active low signal, e.g., RRS/.

Several conventions that can describe the state of a logic signal are: true or false, high or low, one or zero, and active or inactive. In the following description, all logic states are described as high and low. This convention best describes the physical condition of a logic signal and is better suited for troubleshooting.

Frequently, a logic signal is "asserted." If a signal with a trailing slash is asserted, it is low. If a signal without a trailing slash is asserted, it is high. Thus, asserted means that a signal is in its active state.
PS/2 to B Board Interface

The PS/2 to B Board Interface consists of the:

- PS/2 Bus Interface
- Memory and I/O Mapped Control Decoder

Refer to Figure 21 on page 6-9 as necessary.

PS/2 Bus Interface

The PS/2 Bus Interface consists of the circuitry shown on sheet 2 of the B Board schematics. The interface consists of:

- a Data Bus Interface
- an Address Bus Interface
- a Control Interface

Data Bus Interface

The Data Bus Interface consists of bidirectional bus transceivers located at X31Y138 (least significant byte) and X31Y127 (most significant byte). PCRD (PC Read) controls the direction of data flow through the chips. Except when the PS/2 is reading WIDE WORD data or status, PCRD is high, causing PCD0-PCD15 to drive the DAT0-DATF lines, respectively.

Address Bus Interface

The Address Bus Interface consists of line receivers X31Y160 and X31Y149, and part of PAL B1 located at X31Y114. These devices buffer their inputs and provide the high fan-out required to drive the B Board's address bus. X31Y160, driven by PCA0-PCA7, drives the least significant byte of the B Board's address bus (ADR0-ADR7). X31Y149, driven by PCA8-PCA15, drives ADR8-ADR15, respectively. PCA16, the PS/2's MSB address input, is driven by a section of PAL B1. The PAL buffers its pin 2 input and outputs the signal on its pin 23 (ADR10). This section of B1 is functionally identical to any section of line drivers X31Y160 or X31Y149.
Control Interface

The Control Interface consists of PAL B1, except the PCA16 input and its associated ADR10 output. PCINT/ (PC Interrupt) is the only output control signal to the PS/2. The following signals are inputs from the PS/2:

- PCIOW/ (PC I/O Write)
- PCIOR/ (PC I/O Read)
- PCMEMW/ (PC Memory Write)
- PCMEMR/ (PC Memory Read)
- PCBHEN/ (PC Byte High Enable)
- PCRST/ (PC Reset)

Refer to the PAL equations for PAL B1 in the Reference section of this manual. The internal signal called RDY (Ready) goes high if PCIOR/, PCIOW/, PCMEMW/ or PCMEMR/ is asserted (goes low). Thus, RDY goes high about 15 nsec (propagation delay) after these read/write control signals go low. The internal signal called DS (Delayed Strobe) goes high about 15 nsec after RDY goes high. Therefore, DS goes high about 30 nsec after PCIOR/, PCIOW/, PCMEMR/ or PCMEMW/ goes low.

MEMW/ and IOW/ are generated by ANDing inverted PCMEMW/ and inverted PCIOW/, respectively, with DS. This adds an additional 15 nsec of delay; the total is about 45 nsec. MEMW/ and IOW/ generate FIFO load strobos that store data in their respective FIFO(s) on their rising trailing edges. Data must be stable at least 15 nsec prior to the rising edge (setup time) and must remain stable until the rising edge occurs (0 nsec hold time). Timing Diagram 13 on the next page shows this timing.

IOR/ and MEMR/ are generated by ORing DS with PCIOR/ and PCMEMR/, respectively, which results in a stretched IOR/ and MEMR/. This allows the read strobos generated from these signals to go true as soon as possible and remain asserted until after the PS/2's read cycle is completed. This is necessary because the PS/2's read process is not interlocked.

BHEN/ is generated by buffering PCBHEN/. Thus, BHEN/ lags its input by about 15 nsec. BHEN/ is low (active) during all 16-bit transfers, and 8-bit transfers to odd numbered addresses (PCA0 is high). That is, when BHEN/ is low, the data on PCD8-PCD15 (upper byte) is valid.
Timing Diagram 13. PS/2 Interface Timing
INIT/ (Initialize) initializes the Dataram memory. For proper initialization, INIT/ must be asserted for least 1.7 usec. INIT/ is generated by latching PCRST/ on the rising edge of FI. The PS/2 asserts PCRST/ only during its power-up sequence. FI (generated by the A Board every 1/30 second) clocks a D-type latch in B1 that latches PCRST/. The latch’s output is INIT/. Because FI occurs every 1/30 second when the Dataram chassis is powered up, INIT/ has a guaranteed duration of at least 1/30 second.

When powering up the WWW, power up the Dataram chassis before powering up the PS/2. Otherwise, the PCRST/ pulse will end before PAL B1 is powered up and able to capture it.

Memory and I/O Mapped Control Decoder

The Memory and I/O Mapped Control Decoder is shown on sheet 3 of the schematics. This section consists of:

- PAL B2 located at X35Y105
- PAL B3 located at X35Y92
- PAL B4 located at X10Y97
- 4-bit comparator X33Y83
- 4-bit D-type latch X35Y83

PALs B2 and B3 generate memory mapped control signals; PAL B4 generates I/O mapped control signals. IOW/ is applied to PAL B2 (pin 13) because the FIFOs driven by LDF2-LDF5 are loaded with Read-Modify-Write WIDE WORD parameters prior to executing a Mode 3 memory cycle (WIDE WORD Erase). LDF2-LDF5 are I/O mapped during Mode 3 usage. For Modes 0-2, these signals are memory mapped. Table 29 on the next two pages defines the memory and I/O mapping.

WLG, the 4-bit comparator output, is used in the generation of LDF0-LDFE and FA/ in Mode 0. It ensures that only one FIFO write strobe is generated for each address. WLG must be low to generate a Mode 0 Write Data FIFO load strobe. Regardless of the Mode, ALC/ goes low while the PS/2 writes to the Write Data FIFOs. On its rising trailing edge, ALC/ clocks the 4-bit latch located at X35Y83. That is, ALC/ latches the current state of the 4 LSBs of the address bus at the end of the PS/2’s read or write cycle. At this time, the latch’s outputs, which drive the comparator’s B inputs, match the comparator’s A inputs. This causes the A=B output of the comparator to go high, inhibiting any additional write strobes to the same FIFO. NDFF/ (No Data Flag) forces WLG low for the first write to an empty FIFO.
## Table 29. Memory and I/O Map

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<tr>
<th>Signal</th>
<th>Mem/IO</th>
<th>Address</th>
<th>BHEN</th>
<th>Data Transfer Mode</th>
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<td>Mem</td>
<td>Y = 0</td>
<td>X</td>
<td>Mode 0</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = 0</td>
<td>X</td>
<td>Mode 1</td>
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<td></td>
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<td>Mode 2</td>
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<td>Y = 0</td>
<td>0</td>
<td>Mode 1</td>
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<tr>
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<td>Mode 2</td>
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<td>X</td>
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<td>Mode 2</td>
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<td>Y = A</td>
<td>0</td>
<td>Mode 0</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = A</td>
<td>0</td>
<td>Mode 1</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = A</td>
<td>0</td>
<td>Mode 2</td>
</tr>
<tr>
<td>LDFC</td>
<td>Mem</td>
<td>Y = C</td>
<td>X</td>
<td>Mode 0</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = C</td>
<td>X</td>
<td>Mode 1</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = C</td>
<td>X</td>
<td>Mode 2</td>
</tr>
<tr>
<td>LDFD</td>
<td>Mem</td>
<td>Y = C</td>
<td>0</td>
<td>Mode C</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = C</td>
<td>0</td>
<td>Mode 1</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = C</td>
<td>0</td>
<td>Mode 2</td>
</tr>
<tr>
<td>LDFE</td>
<td>Mem</td>
<td>Y = E</td>
<td>X</td>
<td>Mode 0</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = E</td>
<td>X</td>
<td>Mode 1</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = E</td>
<td>X</td>
<td>Mode 2</td>
</tr>
<tr>
<td>FAI/</td>
<td>Mem</td>
<td>Y = E</td>
<td>0</td>
<td>Mode 0</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = X</td>
<td>0</td>
<td>Mode 1</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = X</td>
<td>X</td>
<td>Mode 2</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>Y = X</td>
<td>X</td>
<td>Mode 3</td>
</tr>
<tr>
<td>UBS</td>
<td>Mem</td>
<td>Odd</td>
<td>X</td>
<td>Mode 2</td>
</tr>
<tr>
<td>ALC/</td>
<td>Mem</td>
<td>All</td>
<td>X</td>
<td>All</td>
</tr>
<tr>
<td>RR0/</td>
<td>Mem</td>
<td>Even</td>
<td>X</td>
<td>Mode 1</td>
</tr>
<tr>
<td>RR1/</td>
<td>Mem</td>
<td>Odd</td>
<td>0</td>
<td>Mode 1</td>
</tr>
<tr>
<td>UAW/</td>
<td>I/O (Wr)</td>
<td>Port 33EH</td>
<td>0</td>
<td>NA</td>
</tr>
<tr>
<td>CMW/</td>
<td>I/O (Wr)</td>
<td>Port 33CH</td>
<td>0</td>
<td>NA</td>
</tr>
<tr>
<td>MSIZ/</td>
<td>I/O (Rd)</td>
<td>Port 33CH</td>
<td>0</td>
<td>NA</td>
</tr>
<tr>
<td>STAT/</td>
<td>I/O (Rd)</td>
<td>Port 33EH</td>
<td>0</td>
<td>NA</td>
</tr>
<tr>
<td>MSL/</td>
<td>I/O (Wr)</td>
<td>Port 336H</td>
<td>0</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>I/O (Wr)</td>
<td>Port 336H</td>
<td>1</td>
<td>NA</td>
</tr>
</tbody>
</table>

Table 29 (Continued). Memory and I/O Map
Timing Diagram 14. B Board to A Board Address Transfers
B Board to A Board Interface

The B Board to A Board Interface consists of a Data Bus Interface, an Address Bus Interface and an Interface Control.

Data Bus Interface

The Data Bus Interface consists of the 6 FIFOs shown on sheet 5 of the schematics. These FIFOs are the A Board Data FIFOs which are loaded by individual load strobes from the A Board FIFO Load Strobe Generator (see PAL B5 on sheet 4). For unloading purposes, the A Board Data FIFOs are organized as lower and upper banks. The lower bank consists of X19Y1, X23Y1 and X27Y1; the upper bank consists of X19Y16, X23Y16 and X27Y16. All lower bank FIFOs are unloaded simultaneously when LFR (Lower FIFO Read) goes low; all upper bank FIFOs are unloaded simultaneously when UFR (Upper FIFO Read) goes low. These unload signals are shown in Timing Diagram 14 on the adjacent page.

A Board data words may be one, two or three bytes in length. However, an entire bank of A Board Data FIFOs is read simultaneously, presenting a 24-bit data word (UFD00-UFD17) to the A Board input data latches. UFD10-UFD17 are invalid for 16-bit words; UFD08-UFD17 are invalid for 8-bit words.

Regardless of the word length downloaded from the PS/2, each FIFO within a bank must be written to an equal number of times to prevent data skewing. For example, suppose the PS/2 writes a Blink Rate to the A Board. The Blink Rate is an 8-bit word written to address 00F00H. The PS/2 converts the Blink Rate from an 8-bit to a 16-bit word by combining the Blink Rate with an upper byte of 00H.

By forming the word into a 16-bit word, BHEN/ is asserted when the PS/2 writes to the B Board. BHEN/ must be asserted to qualify FL6 which strobes the Blink Rate's destination address (00F00H) into the A Board Address FIFOs. At this time, FL0, FL2 and FL4 are also asserted (refer to the A Board FIFO Load Strobe Generator description on page 7-12). Thus, each lower bank data FIFO is loaded with the data present at its D-inputs. DAT0-DAT7 contain the 8-bit Blink Rate; DAT8-DATF contain the 00H that converts the 8-bit word to a 16-bit word. Since both X19Y1 and X27Y1 are driven by DAT0-DAT7, they are loaded with the Blink Rate.
X23Y1's D-inputs are driven by BP0-BP7. This bus originates on sheet 7 of the schematics. There, BP0-BP7 are driven by DAT0-DAT7 or DAT8-DATF via the two data selectors located at X17Y73 and X14Y73. The select pin of those data selectors is driven by NAND gate X6Y11B. DBS/ (Double Byte Select), one of the NAND gate's inputs, goes low if BHEN/ is asserted and the address is between 00000 and 03FFFH inclusive. Since the Blink Rate's destination address (00F00H) falls within this range and it is a 16-bit word, DBS/ goes low, causing the NAND gate's output to go high. This selects DAT8-DATF to drive BP0-BP7, respectively. Therefore, for this example, A Board Data FIFO X23Y1 stores 00H.

All transfers to A Board addresses 00000-03FFFH are transferred by the PS/2 as 16-bit data words even if the A Board uses only eight of the bits. As described above, the least significant byte is stored in FIFO X19Y1; the most significant byte is stored in FIFO X23Y1; FIFO X27Y1 has filler data stored in it. All three FIFOs are output to the A Board simultaneously. For information on A Board Data FIFO loading for other address ranges, see Table 31 on page 7-13.

Address Bus Interface

The Address Bus Interface is located on sheet 4 of the schematics. This section consists of the circuitry in these blocks of Figure 21:

- A Board Address FIFOs
- A Board Upper Address Port

A Board Address FIFOs

The A Board Address FIFOs are shown on sheet 4 of the schematics, and consist of the two 4K by 9-bit FIFOs located at X27Y31 and X23Y31. Part of PAL B5 generates the two MSBs of the A Board address and a control signal called DBS/. The remainder of PAL B5 is the A Board FIFO Load Strobe Generator which is described later.

ADR1-ADR3 provide the address inputs for UFA01-UFA0F, respectively. PAL B5 provides the inputs for UFA10 and UFA11 via its pins 23 and 22, respectively. PAL B5 uses the outputs of X14Y24, the A Board Upper Address Port, to determine UFA10 and UFA11. Note that ADR0 is not stored and does not directly drive UFA00 which is an output of PAL B6 located at X8Y23. UFA00 is output twice during each transfer to the A Board, first as a low and then as a high. Thus, each stored address (UFA01-UFA11) represents two consecutive destination addresses.
FL6, an output of PAL B5, loads the A Board Address FIFOs when it goes low. FL6 goes low with MEMW/ if ADR10 is low (A Board destination) and BHEN/ is asserted (16-bit transfer or 8-bit transfer when ADR0 is high). Because each stored address is part of two consecutive addresses, A Board Address FIFO unloading occurs at one-half the rate of the A Board Data FIFO unloading. Timing Diagram 14 shows this relationship.

The A Board Address FIFOs are unloaded by LFR (Lower FIFO Read) which is generated by PAL B6 and shown in Timing Diagram 14. Note that UFA01-UFA11 become valid about 50 nsec after LFR goes low (access time specification). These FIFOs normally enter a tri-state condition when their pin 15 is high. However, because these FIFOs are driving CMOS latches on the A Board, their output loading is very low and primarily capacitive. The capacitance acts as a storage network, stretching the Valid Address duration (see Timing Diagram 14).

The address input latches on the A Board (X57Y36 and X53Y38 - see sheet 2 of the A Board schematics) must always be replaced with identical part numbers when troubleshooting that section of the A Board. If lower input impedance devices are used (e.g., replacing a 74FCT374 with a 74S374), the address outputs of the A Board Address FIFOs may enter the tri-state condition too soon after LFR goes high. Then, the rising edge of DLS that occurs when UFA00 is high may occur after the UFA01-UFA11 address lines become invalid.

The A Board Address FIFOs are reset at the vertical field rate (1/30 second) to ensure that these FIFOs are cleared out periodically. The FIFOs are reset by the B sections of two D-type latches located at X10Y27 and X4Y11. Statically, RRFR/ (Raster Read FIFO Reset) is high, making X10Y27B's pin 12 input high. At this time, X10Y27B's pin 9 output is low. The rising trailing edge of FI clocks X10Y27B, driving its output high. The next rising edge of HPC clocks X4Y11B, driving RRFR/ low. This asynchronously resets X10Y27B, returning its output low. Finally, the next rising edge of HPC clocks X4Y11B, returning RRFR/ to its static high condition. RRFR/ goes low for one HPC period (about 80 nsec) at the beginning of each vertical field.
Prior to writing data to the A Board, the upper two bits of the 18-bit address are programmed by writing to I/O port 336H. The upper two bits function as a page address, i.e., they select a 64K-word address block (page). As long as an A Board address falls within the current page, the Upper Address Port does not require reprogramming prior to writing to the A Board. Writing to I/O port 336H latches the lower four bits of the data bus (DAT0-DAT3) into X14Y24.

X14Y24 passes its latched DAT0-DAT3 outputs to PAL B5 which interprets these inputs, and outputs the MSB and second MSB of the A Board Address on its pins 22 and 23, respectively. Table 30 below shows the interpretation of the output of the Upper Address Port.

<table>
<thead>
<tr>
<th>DAT3</th>
<th>DAT2</th>
<th>DAT1</th>
<th>DAT0</th>
<th>Pin 22</th>
<th>Pin 23</th>
<th>A Board Addresses</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00000-0FFFFFH</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>10000-1FFFFFH</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>D.C. Red</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>D.C. Green</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>10000-1FFFFFH</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>D.C. Blue</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>20000-2FFFFFH</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>30000-3FFFFFH</td>
</tr>
</tbody>
</table>

Table 30. A Board Upper Address Port Interpretation

Control Interface

The Control Interface consists of PALs B5 and B6 located at X20Y46 and X8Y23, respectively. PAL B5 is the A Board FIFO Load Strobe Generator. For more information on PAL B5, see the Reference section of this manual. PAL B6 controls the B Board to A Board Interface. It is described by Timing Diagram 14 and its PAL equations located in the Reference section of this manual.

A Board FIFO Load Strobe Generator

The A Board FIFO Load Strobe Generator drives the FL0-FL6 FIFO load strobes. FL6 loads the A Board Address FIFOs and is described in that section. FL0, FL2 and FL4 load the lower bank FIFOs; FL1, FL3 and FL5 load the upper bank FIFOs. Table 31 defines the load strobe generation as a function of the A Board address.
<table>
<thead>
<tr>
<th>A Board Addresses</th>
<th>Load Strobes</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 336H = 0</td>
<td>FL0, FL2, FL4, FL6</td>
<td>Channel Start Addresses, Panel Switch Points, Display Mode, Blink Rate,</td>
</tr>
<tr>
<td></td>
<td>FL1, FL3, FL5, FL6</td>
<td>Channel Masks, Channel Zoom Factors, Label Numbers, Cursor Parameters</td>
</tr>
<tr>
<td>04000-05FFF</td>
<td>FL0, FL2, FL4</td>
<td>Labels (Even Address)</td>
</tr>
<tr>
<td></td>
<td>FL1, FL3, FL5, FL6</td>
<td>Labels (Odd Address)</td>
</tr>
<tr>
<td>07000-07FFF</td>
<td>FL0, FL1</td>
<td>Graphics Red</td>
</tr>
<tr>
<td>08000-08FFF</td>
<td>FL2, FL3</td>
<td>Graphics Green</td>
</tr>
<tr>
<td>09000-09FFF</td>
<td>FL4, FL5, FL6</td>
<td>Graphics Blue</td>
</tr>
<tr>
<td>0A000-0AFFF</td>
<td>FL0, FL1</td>
<td>Image 1 Red</td>
</tr>
<tr>
<td>0B000-0BFFF</td>
<td>FL2, FL3</td>
<td>Image 1 Green</td>
</tr>
<tr>
<td>0C000-0CFFF</td>
<td>FL4, FL5, FL6</td>
<td>Image 1 Blue</td>
</tr>
<tr>
<td>0D000-0DFFF</td>
<td>FL0, FL1</td>
<td>Image 2 Red</td>
</tr>
<tr>
<td>0E000-0EFFF</td>
<td>FL2, FL3</td>
<td>Image 2 Green</td>
</tr>
<tr>
<td>0F000-0FFF</td>
<td>FL4, FL5, FL6</td>
<td>Image 2 Blue</td>
</tr>
<tr>
<td>Port 336H = 1</td>
<td>FL0, FL1</td>
<td>Dual Channel Red</td>
</tr>
<tr>
<td>00000-0FFFF</td>
<td>FL2, FL3</td>
<td>Dual Channel Green</td>
</tr>
<tr>
<td>Port 336H = 3</td>
<td>FL4, FL5, FL6</td>
<td>Dual Channel Blue</td>
</tr>
<tr>
<td>00000-0FFFF</td>
<td>FL0, FL2, FL4</td>
<td>Cursor 0 Construct</td>
</tr>
<tr>
<td></td>
<td>FL1, FL3, FL5, FL6</td>
<td></td>
</tr>
<tr>
<td>Port 336H = 5</td>
<td>FL0, FL2, FL4</td>
<td>Cursor 1 Construct</td>
</tr>
<tr>
<td></td>
<td>FL1, FL3, FL5, FL6</td>
<td></td>
</tr>
</tbody>
</table>

Table 31. Load Strobe Generation
B Board to Dataram Memory Interface

The B Board to Dataram Memory Interface is shown on sheets 6 through 22 of the B Board schematics and consists of the:

- Write Address/Mode FIFO
- WIDE WORD Upper Address Port Latch
- Mode Latch
- WIDE WORD Address Generator/Latch

Write Address/Mode FIFO

The Write Address/Mode FIFO is shown on schematic sheet 7. It consists of four cascaded 9-bit by 512-word FIFOs located at X17Y82, X14Y82, X12Y82 and X10Y82. Each FIFO drives eight address output lines. The D8/Q8 sections of three of the FIFOs store one of three control signals that must accompany each address.

All FIFOs are loaded simultaneously by PAL B2. It is shown on sheet 3 of the schematics. It goes low when writing to addresses 010000H-01FFFFH and the Mode is 0, 2 or 3, or when BHEN/ is asserted and the Mode is 1.

The Write Address/Mode FIFOs are unloaded when FR/ (FIFO Read) goes low. FR/ is an output of the Cycle Control Logic section. See page 7-35 and sheet 10 of the schematics for more information about FR/.

All Write Address/Mode FIFOs are reset when INI/ goes low. INI/ goes low after about 4.25 seconds of inactivity between the PS/2 and the Dataram memory. Refer to the Write Data FIFO description that starts on page 7-38 for more information on the generation of INI/

The D0-D7 inputs of X17Y82 are driven by ADR0-ADR7, respectively. ADR0-ADR3 function as a byte address. The Q0-Q3 outputs that result from these inputs form the FA (FIFOed Address) bus. FA00-FA03 are used by the Dataram Control and Byte Select Logic to select the byte to be modified in the Mode 2 R-M-W cycle. AC00-AC03 are the 4 LSB inputs to the WIDE WORD Address Generator/Latch. AC1C, the Q8 output of X17Y82, is used as an up/down direction control by the WIDE WORD Address Generator/Latch. The D8 input that generates AC1C is an output of X8Y74, the Mode Latch. When a high is latched into the D1/Q1 section of X8Y74, and the B Board mode is 1 or 3 (see Table 27 on page 6-25), the Address Generator counts up.
AC04-AC0B are the fifth through the twelfth LSB inputs to the WIDE WORD Address Generator/Latch. They are driven by ADR8-ADRF, respectively. The D8/Q8 section of X14Y82 stores MC0 (Mode Control 0), the LSB of the 2-bit B Board mode code (see Table 27).

AC0D-AC13 are the thirteenth through the twentieth LSB inputs to the Address Generator/Latch. The inputs for these outputs are driven by the 8 LSB outputs of the WIDE WORD Upper Address Port Latch. MC1, the Q3 output of the Mode Latch, drives the D8/Q8 section of X12Y82. FMC1, the Q8 output of X12Y82 is the MSB of the 2-bit B Board mode code (see Table 27).

AC14-AC1B are the twenty-first through the twenty-eighth LSB inputs to the WIDE WORD Address Generator/Latch. The inputs for these outputs are driven by the 8 MSB outputs of the WIDE WORD Upper Address Port Latch.

**WIDE WORD Upper Address Port Latch**

The WIDE WORD Upper Address Port Latch is shown on sheet 7 of the schematics. It consists of the two octal D-type latches located at X17Y108 and X17Y97. These latches latch the 16 data bus bits on the rising trailing edge of UAW (Upper Address Write) which is asserted by writing to I/O port 33E\text{H}. The data stored by the two latches functions as a page address. The page size is 4096 WIDE WORDs (65536 bytes).

**Mode Latch**

The Mode Latch is shown on sheet 7 of the schematics and consists of the 4-bit D-type latch located at X8Y74. This latch stores the DAT8-DATB data on the rising trailing edge of CMW (Change Mode Write). CMW is asserted by writing to I/O port 33C\text{H}. The latched DAT8 output (X8Y74's Q1 - pin 2) controls the WIDE WORD Address Generator/Latch's count direction in Modes 1 and 3. The latched DAT9 and DATA outputs (X8Y82 pins 7 and 10, respectively) are the Mode bits. Table 27 defines the Modes. The latched DATB output is not used though it is stored by FIFO X10Y82.
WIDE WORD Address Generator/Latch

Figure 22 on page 6-26 is an expansion of the WIDE WORD Address Generator/Latch block shown in Figure 21. All circuitry for this section is located on sheet 12 of the schematics.

Address Counter and Latch

The Address Counter and Latch consists of the three octal up/down counters located at X4Y44, X4Y57 and X4Y70, and the 4-bit up/down counter located at X4Y35. Together, these fully synchronous cascaded counters provide a 28-bit address input to the Bus Drivers. At all times the counters are either in a parallel load state or a count state. When ACL (Address Counter Load) is low and ACG (Address Counter Gate) is high, the counters are preset to the levels on the AC00-AC1B inputs on the next rising edge of ACC (Address Counter Clock). When ACL is high and ACG is low, the counters increment or decrement on the rising edge of ACC. Refer to the Address Generator Controller section on page 7-27 for more information on ACC, ACL and ACG. Note that AC1C controls the count direction via the up/down pin on each chip.

Address Over Range Protect Logic

The Address Over Range Protect Logic, consisting of most of PAL B10, is shown on sheet 12 of the schematics. It is located at X14Y4.

PAL B10 compares WSZ04-WSZ07 (WSZ08-WSZ10 are not used) with the upper seven active output bits (WAD21-WAD27) of the Address Generator and Latch. The PAL asserts ARE (Address Real Enable) if the address exists. ARE controls the tri-state enable of X2Y72. The Address Over Range Protect Logic is identical to the A Board’s nonexistent memory protection logic provided by PAL A13. The PAL A13 description in the A Board’s WIDE WORD Address Bus Drivers description is also valid for the Address Over Range Protect Logic portion of PAL B10.

Bus Drivers

The Bus Drivers section is shown on sheet 12 of the schematics and consists of four inverting octal bus drivers located at X2Y39, X2Y50, X2Y61 and X2Y72. Each chip has two tri-state output enables, G1 and G2 (pins 1 and 19, respectively). All G1 inputs are wired in parallel and driven by WRA/. WRA/ is asserted while the B Board has access to the Dataram memory (the A Board has finished its Raster Read cycle). The pin 19 inputs of chips X2Y39, X2Y50 and X2Y61 are wired in parallel and driven by WCY which is high only during the power-up clear cycle (about 0.532 seconds per WSA board set installed).
X2Y72 drives WAD21/-WAD27/ which are the seven most significant actively driven address inputs to the WIDE WORD memory (WAD28/-WAD31/ have grounded inputs). The pin 19 input of this chip is driven by ARE, the output of the Address Over Range Protect Logic. The Address Over Range Protect Logic compares the inputs of X2Y72 with WSZ04/-WSZ07/ and asserts ARE if the memory size is large enough for the current address. If the address is too large, ARE is not asserted, X2Y72 is not enabled and the nonexistent address is remapped to an address specified by the remaining three Bus Driver chips.
<table>
<thead>
<tr>
<th>WENSQ</th>
<th>WREAD</th>
<th>WWBW1</th>
<th>WWBO-7 6 5 4 3 2 1 0</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X X X X X X X X X X</td>
<td>Sequential Read</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 1 1 1 1 1 1 1</td>
<td>WIDE WORD Read</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1 1 1 1 1 1 1 1</td>
<td>WIDE WORD Write</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1 1 1 1 1 1 1 1</td>
<td>R-M-W WIDE WORD</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 1 1 1 1 1 1 1</td>
<td>R-M-W Byte 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 1 1 1 1 0 1 1</td>
<td>R-M-W Byte 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 1 1 1 0 1 1 1</td>
<td>R-M-W Byte 2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 1 1 0 1 1 1 1</td>
<td>R-M-W Byte 3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 1 0 1 1 1 1 1</td>
<td>R-M-W Byte 4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 0 1 1 1 1 1 1</td>
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<td>0 1 1 1 1 1 1 1</td>
<td>R-M-W Byte 15</td>
</tr>
</tbody>
</table>

X = Don’t Care

Table 32. Dataram Mode Control Summary
Read/Write Control

The Read/Write Control block shown in Figure 20 consists of the following blocks in Figure 21:

- Dataram Control and Byte Select
- Address Generator Controller
- Subcycle Repeat Counter
- Cycle Control Logic
- Memory Size Buffer
- FIFO Status Port

Dataram Control and Byte Select

The Dataram Control and Byte Select section is shown on sheets 10 and 11 of the schematics. This section consists of Dataram Mode Control Logic, Byte Select Logic and Handshake Control.

Dataram Mode Control

Only four of the 84 explicit modes of memory operation are used. These modes are:

- WIDE WORD Write (Mode 0)
- WIDE WORD Read (Mode 1)
- Read/Modify/Write Byte (Mode 2)
- Read/Modify/Write WIDE WORD (Mode 3 - erase)

Dataram mode selection is accomplished via WENSQ, WREAD/ and WWBW1/. Table 32 on the adjacent page summarizes the Dataram mode control signals.

WENSQ/ is low only during sequential reading or writing. Since sequential read is the only sequential mode used in the WWW and it is used exclusively by the A Board, WENSQ/ is controlled entirely by the A Board. When the B Board has control of the Dataram memory, WENSQ/ is high.
**WREAD/**

WREAD/ is low during reading (Mode 1) and high during writing (Mode 0). It is also low during Read-Modify-Write modes (Modes 2 and 3).

Refer to sheet 10 of the schematics. WREAD/ begins with the generation of WRD by PAL B7. The PAL equations for B7 show that WRD is high during Modes 1, 2 and 3, and while WCY is high. WCY is described in the Handshake Control section. WRD drives the A3 input of line driver X8Y12A shown on sheet 11. The Y3 output of X8Y12A is WREAD/.

**WWBW1/**

WWBW1/ is an output of PAL B7 located at X6Y35 and shown on sheet 10 of the schematics. WWBW1/ is low in Mode 3 and during Mode 2 if FA03 is high. FA03 is high while addressing any byte(s) on the upper half of the 128-bit data bus (bytes 8-15). Therefore, WWBW1/ is low in Mode 3 and while addressing bytes in the upper 64-bit data word during Mode 2. At all other times (Modes 0, 1 and lower word addressing in Mode 2), WWBW1/ is high.

**Byte Select Logic**

WWB00/-WWB07/ select the byte(s) to be modified in non-WIDE WORD modes. These control signals are outputs of PAL B7 located at X6Y35 and shown on sheet 10 of the schematics. These lines are all high during WIDE WORD modes (B Board Modes 0, 1 and 3). In Mode 2 (Read/Modify/Write Byte mode), only one byte select line can be low at one time. Therefore, all byte select lines are high in Modes 0, 1 and 3 while one byte select line is low in Mode 2.

PAL B7 uses FA00-FA02 to address one of the byte select lines (WWB00/-WWB07/) only when Mode 2 is selected. These lines can select a byte on the upper or lower half of the data bus as a function of WWBW1/ (described above).
Handshake Control

The Handshake Control Logic is shown on sheet 11 of the schematics. The four interlocked handshake signals are WADAV/, WADAC/, WDTRQ/ and WDTAC/. WRA/ and WCY are described prior to describing the handshake signals because they are used to gate some of the handshake signals.

When the A Board completes its Sequential Read cycle, it sets WREN/ high. WREN/ remains high until the start of the next scan line. When WREN/ is high, the B Board can access the Dataram memory. It’s possible (and probable) that a Dataram memory cycle can be initiated just prior to the falling trailing edge of WREN/, leaving little or no time for completing the initiated Dataram memory cycle. To allow the last cycle enough time to complete, WREN/ is stretched about 720 nsec.

WREN/ enters the B Board on pin 23 of the JB connector and is buffered by the A4/Y4 section of X8Y1. WRE/, the buffer’s Y4 output, drives the Load input (pin 11) of decade counter X33Y74. While the A Board has control of the Dataram memory, the decade counter is in a count condition (WRA/ is high) but the counter cannot count because its G input (pin 4) is still high from the previous cycle. Refer to Timing Diagram 15 on the next page. When WREN/ and WRE/ go low, the counter enters a Load condition. This drives the counter’s pin 12 low; the counter remains in a Load condition until WRE/ returns high. Then, the counter is allowed to count at the HPC (Half Pixel Clock - see PAL B6 on sheet 4) rate. On the rising edge of the ninth HPC clock pulse, the counter’s pin 12 (WRA/) goes high. When WRA/ goes high, the counter cannot count until it is reloaded again by WREN/. Thus, WRA/ goes low a few nanoseconds after WREN/ goes low and remains low for nine HPC clock pulses (9 x 80 nsec = 720 nsec) after WREN/ goes high.

Refer to sheet 11 of the schematics. Section A1/Y1 of line driver X8Y1 drives inverter X8Y27D with buffered WCBY/. WCY, the inverter’s output, goes high when WCBY/ goes low. WCBY/, the output of AND gate X12Y7A, goes low if WCLBY/ or WMINT/ goes low. WMINT/ is asserted during power-up and remains low until the memory’s +5 volt logic supplies reach minimum operating voltage (a few milliseconds). WCLBY/ goes low while the memory self test is running (about 133 milliseconds per WSA board installed). This test is automatically initiated immediately after power-up. In summary, WCY goes high upon power-up and remains high for about 133 msec per WSA board installed.
Handshake Signals

The Handshake Logic is shown on sheet 11 of the schematics. A memory read or write cycle, and therefore the Handshake Logic, is initiated when GO goes high. GO is an output of the Cycle Control Logic and is explained in that section’s description (page 7-34). Refer to Timing Diagrams 16 and 17 (on the next two pages) throughout this description.

The handshake sequence for Modes 0 and 1 is: WADAV/, WADAC/, WDTRQ/ and WDTAC/; the handshake sequence for Modes 2 and 3 (R-M-W modes) is: WADAV/, WADAC/, WDTRQ/, WDTAC/, WDTRQ/ and WDTAC/.

WADAV/

The rising leading edge of GO clocks the D-type latch located at X10Y3A. This clocks a low into the latch, causing WAV (WIDE WORD Address Available), its pin 6 output, to go high. WAV drives the A1/Y1 section of inverting line driver X8Y12A whose output is WADAV/.

WADAC/

After WADAV/ is asserted, the Dataram responds within a few nanoseconds by asserting WADAC/. The A5/Y5 section of line driver X8Y1 generates WAC/ by buffering WADAC/. WAC/ drives pin 13 of OR gate X8Y42D low when WADAC/ is asserted. This OR gate’s pin 12 is driven low by OR gate X8Y42C because WRA/ and WCY are low (see page 7-21). Thus, OR gate X8Y42D’s output goes low when WADAC/ is asserted. This low output causes the outputs of AND gates X6Y3A and X6Y3B to go low. When X6Y3A goes low, D-type latch X10Y3A is preset, causing its pin 6 output to go low. This ends WADAV/. Note that if INI/ is asserted, X10Y3A is also preset, driving WAV low. For information on INI/, refer to the Write Data FIFO description that begins on page 7-38.

WDTRQ/

The previous paragraph describes how the output of AND gate X6Y3B is driven low. This low output presets D-type latch X10Y3B, causing WDQ to go high. The A2/Y2 section of inverting line driver X8Y12A inverts WDQ to produce WDTRQ/.

The R-M-W modes (Modes 2 and 3) require two WDQ pulses. The first pulse is generated as a result of WADAC/ being asserted as described above. The second WDQ is generated as a result of the first WDTAC/ pulse.
Timing Diagram 16. WIDE WORD Handshake Timing Relationships
Timing Diagram 17. Read-Modify-Write Timing Relationships

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Upon receipt of the WDTRQ/, the Dataram memory either latches the input data (memory write cycle) or fetches the requested data (memory read cycle). Upon completion of the latching or fetching process, the Dataram memory asserts WDTAC/. WDTAC/ is inverted by inverting line driver X8Y12B before being applied to pin 9 of AND gate X6Y3C. Thus, pin 9 of the AND gate goes high when WDTAC/ is asserted. The output of OR gate X8Y42C is low after the power-up and memory self test cycles complete, and the B Board has access to the Dataram memory. This low output is inverted by X6Y27E before being applied to pin 10 of AND gate X6Y3C. WDC, this AND gate's output, goes high when WDTAC/ is asserted. The rising edge of WDC clocks D-type latch X10Y3B, driving WDQ low and ending WDTRQ/.

WDC drives inverter X6Y27C and AND gate X12Y27A. The inverter drives logic that generates the second WDTRQ/ in Modes 2 and 3; the AND gate generates GWDC (Gated WDC). In Modes 2 and 3, GWDC is asserted during the second WDC pulse of the R-M-W cycle; in Modes 0 and 1, GWDC is asserted during the first and only WDC pulse of the transfer cycle. Thus, GWDC is asserted at the completion of the transfer cycle regardless of the transfer mode. GWDC is the Data Acknowledge signal line on Figure 21 that originates in the Dataram Control and Byte Select block and terminates in the Cycle Control Logic block.

Timing Diagram 17 on the previous page shows the timing relationships for a Mode 2 or 3 transfer. The trailing falling edge of the first WDC pulse in a Read-Modify-Write transfer clocks D-type latch X10Y27A via inverter X8Y27C. Statically, this latch is reset, making WLO/ (WIDE WORD Lock Out) and the pin 4 input of AND gate X12Y27B high. In Modes 0 and 1, this AND gate presents a low to the D-input of the latch because FMC1 is low; in Modes 2 and 3, this AND gate passes its high pin 4 input to the latch's D-input because FMC1 is high. Therefore, if the mode is 0 or 1, MWCK is always low after the latch is clocked by WDC; if the mode is 2 or 3, MWCK is always high after the latch is clocked by the first WDC pulse.

When MWCK goes from a low to a high as a result of the first WDC pulse, latch X10Y19A is clocked, latching QRST/ into the latch. At this time, QRST/ is high; QD1, QD2 and QD3 are low. QD1 goes high when X10Y19A is clocked by MWCK going high.
On the first rising edge of PXLCK after QD1 goes high, QD2 goes high and QRST/ goes low. When QRST/ goes low, AND gate X12Y27C drives the pin 1 input (Clear) of latch X10Y19A low, clearing the latch and driving QD1 low again. On the second rising edge of PXLCK after QD1 initially went high, QD3 goes high and QD2 goes low. The third rising edge of PXLCK after QD1 initially went high drives DQ/ low, setting latch X10Y3B and asserting WDQ and WDTRQ/ the second time. The resulting WDTAC/ asserts WDC again. The trailing edge of WDC clocks latch X10Y27A again, latching the low out of AND gate X12Y27B into the latch. This returns MWCK to a low level and WLO/ to a high level and completes the transfer. Latches X10Y19B, X10Y11A and X10Y11B delay the start of the second WDTRQ/ by about 120 nsec (3 PXLCK clock periods), which is a timing requirement of the Dataram memory.

Address Generator Controller

The Address Generator and Latch shown on sheet 12 of the schematics requires these three control signals:

- ACG (Address Counter Gate)
- ACL (Address Counter Load)
- ACC (Address Counter Clock)

The Address Generator Controller generates these signals and is shown on sheet 10 of the schematics.

ACG and ACL are complementary outputs of the D-type latch located at X8Y58B. When the latch is set (pin 9 is high and pin 8 is low), the Address Generator and Latch counts on the rising edge of ACC. When the latch is reset, the Address Generator and Latch is preset to its parallel inputs by the rising edge of ACC. The latch’s D-input is driven by FMC0 (LSB of the 2-bit Mode word). Therefore, after being clocked by GO, ACL is the latched level of FMC0, and ACG is the complement of FMC0. That is, for Modes 0 and 2, the Address Generator and Latch is in a load condition and functions as a latch. Modes 1 and 3 cause ACL to be high and ACG to be low. This allows the Address Generator and Latch to count.

The latch at X8Y58B is cleared at the end of Modes 1 and 3 by a low output from NAND gate X8Y50D. This output goes low when the Subcycle Repeat Counter decrements to zero, indicating the requested number of WIDE WORDs were read (Mode 1) or erased (Mode 3).

ACC is an output of the Cycle Control Logic.
Subcycle Repeat Counter

The Subcycle Repeat Counter is shown on sheet 10 of the schematics. It consists of two octal counters located at X6Y70 and X6Y48, and one 4-bit counter located at X6Y61. These counters are synchronous up/down counters that are wired for down counting only. AND gates X8Y34D and X8Y34C, OR gate X8Y42B, and NAND gates X8Y50C and X8Y50D control the Subcycle Repeat Counter.

The three counter chips are cascaded, resulting in a 20-bit down counter. Functionally, however, these counters are treated as two cascaded counters consisting of a 12-bit line length counter and an 8-bit line counter. The line length counter consists of X6Y70 (8 LSBs) and X6Y61 (4 MSBs); the line counter consists of X6Y48.

Write Data FIFO output bits D200-D310 are preload inputs to the line length counter; Write Data FIFO output bits D320-D390 are preload inputs to the line counter. ACL (Address Counter Load) directly drives the load input of the line counter and indirectly drives the line length counter’s load input via AND gate X8Y34C. Thus, both counters are preloaded when ACL goes low. When the line length counter decrements to zero, the RCO output of X6Y61 goes low enabling the line counter and driving the pin 9 input of AND gate X8Y34C low. The resulting low output of AND gate X8Y34C reloads the line length counter. Thus, the line length counter is preloaded by ACL and each time the line length counter decrements to zero; the line counter is preloaded by ACL only.

Both counters are clocked by the rising edge of ACC (Address Counter Clock - see the Cycle Control Logic description). ACC preloads the counters if their respective load pin is low; ACC decrements the respective counter if its count enable pins (CEP - pin 12 and CET - pin 13) are low. If neither the load nor the count enable pins are low, ACC has no effect on the respective counter.

The line length counter decrements on the rising edge of ACC if ACL is high and ACG is low (see the description for D-type latch X8Y55B in the Cycle Control Logic section). Upon reaching zero, the RCO output of X6Y61 goes low, driving the count enable input of the line counter low. On the next rising edge of ACC, the line counter decrements and the line length counter is preset to the line length input.
Control of the Subcycle Repeat Counter is accomplished by controlling ACG and ACL. These signals are generated by D-type latch X8Y58B. This chip, with the exception of the clear input (pin 13), is described in the Cycle Control Logic section below. Therefore, Subcycle Repeat Counter control consists of analyzing the clear input to X8Y58B.

Prior to the start of each Dataram memory read or write cycle, X8Y58B is reset as a result of the completion of a previous read or write cycle. For Modes 0 or 2, X8Y58B remains reset because a low (FMCO) is clocked into it when GO goes high. Modes 1 and 3 cause X8Y58B to be set, causing the line length counter to be enabled (ACG is low). This causes the line length counter to decrement on the rising edge of each ACC pulse.

Until the line length counter reaches zero, the high RCO output of X8Y61 causes the output of OR gate X8Y42B to be high. During Modes 2 and 3, the FMC1 input to this OR gate causes its output to be high for the entire cycle. Thus, the pin 9 input to NAND gate X8Y50C is high all times except while reloading the line length counter in Mode 1.

The pin 10 input of NAND gate X8Y50C is driven by AND gate X8Y34D. This AND gate passes the TC (Terminal Count - pin 14) status of the line counter to NAND gate X8Y50C in Modes 1 and 3 because FMCO is high in these modes. In Modes 0 and 2, the output of AND gate X8Y34D is low. NAND gate X8Y50C combines the outputs of OR gate X8Y42B and AND gate X8Y34D to produce an output that is high in Modes 0 and 2, low in Mode 1 except during line length counter reloading or when the line counter reaches its terminal count, and low in Mode 3 except when the line counter reaches its terminal count.

GWDC (Gated WIDE WORD Data Accepted) is an output of the Handshake Control Logic. GWDC lags WDC by a few nanoseconds in Modes 0 and 1; it lags the second WDC pulse in a R-M-W cycle (Modes 2 and 3) by a few nanoseconds. Thus, the rising edge of GWDC, regardless of mode, indicates the end of a word transfer. NAND gate X8Y50D combines GWDC with the output of NAND gate X8Y50C to produce an output that goes low during each GWDC pulse in Modes 0 and 1, and during the last GWDC pulse in Modes 2 and 3. The low output from NAND gate X8Y50D, in addition to clearing D-type latch X8Y58B, clears latch X8Y58A via AND gate X12Y7B.
Timing Diagram 18. WIDE WORD Write (Mode 0) Timing
Timing Diagram 19. WIDE WORD Mode 1 (Readback RAM) Timing

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Timing Diagram 20. Read-Modify-Write Byte (Mode 2) Timing
Timing Diagram 21. WIDE WORD Erase (Mode 3) Timing
Cycle Control Logic

The Cycle Control Logic is shown on sheets 10 and 11 of the schematics. Timing Diagrams 18 through 21 on the previous pages describe the control timing relationships for Modes 0-3, respectively. Refer to these diagrams as necessary.

The Cycle Control Logic generates GO each time a Dataram memory read or write transfer is executed. Multiple sequential reads are usually executed in Mode 1; multiple sequential erases are usually executed in Mode 3. For these modes, the Cycle Control Logic must generate GO as rapidly as the Dataram memory can execute a transfer until the required number of WIDE WORDs is either transferred or erased. A Mode 0 or Mode 2 cycle always consists of a single GO signal per cycle. The logic that generates GO consists of:

- AND gate X8Y34A
- AND gate X8Y34B
- NAND gate X8Y50A
- NAND gate X8Y50B
- D-type latch X8Y58A
- D-type latch X8Y66A
- D-type latch X8Y66B

GO is the latched output of D-type latch X8Y66A; it lags ACC (Address Counter Clock) by one clock period (40 nsec). ACC goes high on the first rising edge of PXLCK following a high output from AND gate X8Y34B. For this AND gate to have a high output, its pins 4 and 5 must be high. Pin 4, driven by AND gate X8Y34A, is high if the Dataram memory isn't busy (MBSY/ is high) and the B Board has control of the memory (WREN is high). MBSY/ is asserted in response to WADAV/ going low and remains asserted until the memory can again be accessed.

The pin 5 input to AND gate X8Y34B is low prior to the start of a memory read or write cycle. This input is controlled by ALC/ and DFE/. ALC/ is an output of PAL B3 shown on sheet 3 of the schematics. It goes low any time data is written to the Write Data FIFOs (MEMW/ is low and ADR10 is high). DFE/ goes low when the last address queued in the Write Address/Mode FIFO is read. Thus, the output of NAND gate X8Y50A is high while the PS/2 is writing into the Write Data FIFOs or the Write Address/Mode FIFOs, or the Write Address/Mode FIFOs are empty.
When neither ALC/ nor DFE/ is asserted, NAND gate X8Y50A has a low output. This output is NANDed with FR/ by NAND gate X8Y50B. FR/is high as a result of the clear input (pin 1) generated at the end of the previous write cycle. Therefore, when pin 4 of NAND gate X8Y50B goes low, its output goes high. The next rising edge of PXLCK latches the high output of NAND gate X8Y58A into D-type latch X8Y58A. This causes FR/ to go low and the pin 5 input to AND gate X8Y34B to go high. Once FR/ goes low, the output of NAND gate X8Y50B stays high regardless of the output of NAND gate X8Y50A. Thus, once D-type latch X8Y58A is set, it remains set until it is cleared by an output from AND gate X12Y7B.

The high output of NAND gate X8Y34B is latched by D-type latch X8Y66B, causing ACC to go high. For single transfer modes and the first transfer of multiple transfer modes, ACC loads the Write Address/Mode FIFO outputs into the WIDE WORD Address Generator/Latch and loads the D200-D390 outputs of the Write Data FIFO into the Subcycle Repeat Counter. Forty nanoseconds after ACC goes high, GO goes high, clocking X8Y58B. X8Y58B puts the WIDE WORD Address Generator/Latch and Subcycle Repeat Counter into the load state (Modes 0 or 2) or count state (Modes 1 or 3) as a function of FMC0.

A few nanoseconds after GO is asserted, WADAV/ is asserted, causing the Dataram memory to assert MBSY/. MBSY/ remains asserted until the memory can respond to the next transfer request. MBSY/, an input to AND gate X8Y34A, causes the output of AND gates X8Y34A and X8Y34B to go low when it goes low. Two PXLCK periods later, GO goes low. For all modes, the pin 5 output of latch X8Y58A remains high until the last transfer in the cycle is completed. Therefore, AND gate X8Y34B goes high immediately after MBSY/ returns high. On the next rising edge of the PXLCK clock pulse, ACC goes high, clocking the WIDE WORD Address Generator/Latch and decrementing the Subcycle Repeat Counter. Forty nanoseconds later, GO is asserted again. This process repeats until the Subcycle Repeat Counter reaches zero, clearing latch X8Y58A. This blocks the generation of additional GO strobes until FR/ is driven low again.
Memory Size Buffer

The Memory Size Buffer is shown on sheet 6 of the schematics and consists of inverting line drivers X2Y17 and X2Y28.

The Dataram memory passes available memory information to the B Board on its WSZ00/-WSZ11/ (WIDE WORD Size) bus. The WSZ00/-WSZ11/ lines are the binary representation of the total number of 128K word blocks of memory available. WWWs can have up to 32 megawords of memory which equates to 256, 128K word blocks. This requires memory size lines WSZ00/-WSZ07/ to represent the maximum available memory. The remaining lines (WSZ08/-WSZ11/) are used only when multiple units are daisy chained together. Since WIDE WORD chassis are always single units, WSZ08/-WSZ11/ are always inactive high.

Inverting line drivers X2Y17 and X2Y28 drive the DAT bus with the active low WSZ bus lines when they are enabled by MSIZ/ (port 33CH Read). WSZ00/-WSZ11/ drive DAT0-DATB, respectively. In addition to the memory size information passed to the PS/2 via the Memory Size Buffer, CFE/, CHF/, DFE/ and DHF/ are passed to the PS/2 via DATC-DATF, respectively. CFE/ and CHF/ are the A Board Address FIFO’s empty and half-full status signals, respectively; DFE/ and DHF/ are the Write Address/Mode FIFO’s empty and half-full status signals, respectively. Thus, these four status signals are functionally part of the FIFO Status Port.
FIFO Status Port

The FIFO Status Port is shown on sheet 6 of the schematics and consists of an octal tri-state line driver located at X2Y6.

The remaining components on sheet 6, except X2Y17 and X2Y28, combine 28 FIFO status flags into seven line driver inputs. The remaining line driver input is used as a Mode 1 Complete flag.

The FIFO Status Port is enabled onto the lower half of the DAT bus (DAT0-DAT7) when STAT/ is asserted (port 33EH Read). The A1-A3 (pins 2-4) inputs to the FIFO Status Port are driven by three 2-input NAND gates located at X4Y3A, X4Y3B and X4Y3C, respectively. These NAND gates combine the FIFO Full flag outputs of the six FIFOs making up the A Board Data FIFOs (see sheet 5) into three status inputs to X2Y6. A high on the A1, A2 or A3 inputs indicates one or both FIFOs making up the lower, middle or upper bytes, respectively, of the A Board Data FIFOs are full.

X4Y3D monitors the A Board Address FIFOs (see sheet 4) for a full condition. This NAND gate drives the A4 input of X2Y6.

Two 8-input NAND gates located at X4Y19 and X4Y27 monitor the 16 FIFOs, making up the Write Data FIFO (see sheets 8 and 9) for a full condition. A high on X4Y19 or X4Y27 indicates one or more of the FIFOs monitored by the respective NAND gate are full.

NAND gate X6Y11A monitors the four FIFOs making up the Write Address/Mode FIFO (see sheet 7) for a full condition.

The Mode 1 Complete flag is generated by D-type latch X4Y11A and AND gate X6Y3D. The latch latches the level of RWA/ (Read/Write Address) on the rising trailing edge of FR/. FR/ goes high at the end of each Dataram memory read or write cycle. RWA/ is low only during a Mode 1 cycle. Thus, the latch's pin 6 output goes high at the end of a Mode 1 cycle. Once pin 6 goes high, it stays high until AND gate X6Y3D goes low, presetting the latch. The AND gate's output goes low if RR0/ or RR1/ (Readback RAM Read bits 0 and 1, respectively) is asserted. The PS/2 asserts one or both of these lines to establish the data word length each time the Readback RAM is read. Thus, reading one or more bytes of data from the Readback RAM automatically clears the Mode 1 Complete flag.
Data FIFO

The Data FIFO section shown in Figure 20 consists of the Write Data FIFO block and the Modify Data and Mask Latch block in Figure 21.

Write Data FIFO

The Write Data FIFO section is shown on sheets 8 and 9 of the schematics. The Write Data FIFO operation is Mode dependent. In Mode 0, it assembles 128-bit data words for output to the Dataram memory via the Bus Flippers. In Mode 1, a 20-bit data word, describing the number of WIDE WORDS to be read, is assembled and sent to the Subcycle Repeat Counter. In Mode 2, an 8-bit mask word and an 8-bit data modifier word are assembled and output to the Bus Flippers section. Mode 3 is a combination of Modes 1 and 2. It consists of a 20-bit word describing the number of WIDE WORDS to be erased, an 8-bit mask selecting the bit to be erased within each byte and an 8-bit modifier that sets each masked bit to 1 or 0.

The FIFOs shown on sheet 8 form the lower data bus word (D000-D630); the FIFOs shown on sheet 9 form the upper data bus word (D001-D631). The 0 or 1 in the last digit of the data bus line labels denotes the lower or upper data words, respectively. Mode 0 uses all bits of both bus words (128 bits - D000 through D630 and D001 through D631); Modes 1-3 use parts of the lower bus word only.

With the exception of FIFOs X28Y104 and X25Y104, the FIFOs' D-inputs are driven by DAT0-DAT7 or DAT8-DATF. The D-inputs of X28Y104 and X25Y104 are driven by the multiplexed BP bus (BP0-BPF) that originates on sheet 7. The BP bus is a part of the Modify Data and Mask Latch section. Refer to that section for more information.

Regardless of the mode, each of the 16 FIFOs must have its load line strobed before beginning the next word or command load. Those FIFOs, whose data is unused in Modes 1, 2 or 3 (e.g., Mode 1 uses only 20 bits), must be loaded with filler data because loading a FIFO also increments the internal address pointers. If each FIFO isn’t loaded an equal number of times, data skewing will occur during unloading since all FIFOs are unloaded simultaneously when FR/ goes low.
In Mode 0, each FIFO is loaded with one byte of the 12-bit data word. FIFO X28Y104 is loaded with the LSB (byte 0); X20Y59 is loaded with the MSB (byte 16). LDF0-LDFE store bytes 0-14, respectively; FAL stores byte 15 and the address (see sheets 8 and 9 to associate the FIFO with the byte stored).

In Mode 1, D4-D7 of FIFO X23Y104, D0-D7 of FIFO X20Y104 and FIFO X28Y89 are loaded with the preset value for the line length counter section of the Subcycle Repeat Counter. The remaining FIFOs and the D0-D4 inputs to FIFO X23Y104 are loaded with filler data.

In Mode 2, BP0-BP7 (D-inputs to FIFO X28Y104) supply the data modifier and BP8-BPF (D-inputs to FIFO X25Y104) supply the mask to the Write Data FIFO. The remaining FIFOs are loaded with filler data.

In Mode 3, FIFOs X28Y104 and X25Y104 are loaded as described for Mode 1 above; FIFOs X23Y104, X20Y104 and X28Y89 are loaded as described for Mode 2. The remaining FIFOs are loaded with filler data.

Table 29 on pages 7-6 and 7-7 describes the generation of LDF0-LDFE and FAL. Each signal drives a FIFO load strobe via a 100-ohm damping resistor. FIFOs can be loaded individually since each FIFO has its own load strobe. All Write Data FIFOs are unloaded simultaneously by FR/ which is applied to the Read input (pin 15) of each FIFO via a 47-ohm damping resistor. For more information on FR/, refer to the Cycle Control Logic description.

Each of the 16 FIFOs making up the Write Data FIFO section provides a FIFO Full status bit to the Write Data FIFO status bus (WFD0-WFDF). This bus provides Write Data FIFO status to the Status Port; see NAND gates X4Y19 and X4Y27 on sheet 6 of the schematics.

The lower word Write Data FIFOs are reset by PAL B9 located at X31Y76; the upper word Write Data FIFOs are reset by PAL B9 located at X23Y48. FIFOs are individually reset when GO goes high if the respective FIFO's Q8 output remains high. This indicates a "hung up" FIFO because the grounded D8 input should always result in a low Q8 output when the FIFO is enabled. A high Q8 output when GO is high means the respective FIFO did not come out of its tri-state condition and must be reset.
All FIFOs are simultaneously reset if INI/ goes low. INI/ is generated by the logic shown in the upper right corner of sheet 12 of the schematics. This logic asserts INI/ if about 4.25 seconds pass without the PS/2 writing any data to the Dataram memory. The following paragraphs describe how this is accomplished.

The 8-bit ripple counter, resulting from the two cascaded 4-bit counters located at X31Y68A and X31Y68B, is clocked at a 30 Hz rate by FI. Thus, assuming the counters were initially cleared, the QD output of X31Y68B goes high on the 128th FI pulse. At this time, the high output of AND gate X12Y7C is latched into X31Y60A, driving pin 5 of latch X31Y60A and the D-input of latch X31Y60B high. The next rising edge of FL6 clocks X31Y60B, driving INI/ low. When INI/ goes low, AND gate X12Y7C goes low, clearing latch X31Y60A. This drives the D-input of X31Y60B low again. The next rising edge of FL6 latches this low input, returning INI/ to a high.

FL6 is asserted each time the PS/2 writes address information into the A Board Address FIFOs. This occurs several times during each vertical blanking period. The counters are clocked by FI at the beginning of every other vertical blanking period. Therefore, once the counters reach 128, FL6 causes INI/ to go low during the period between the first and the second address write cycles to the A Board Address FIFOs. This resets the Write Data FIFOs.

If the PS/2 writes to the Dataram memory, ALC/ is asserted. PAL B10 inverts the ALC/ input to its pin 18, causing its pin 19 to go high. This output clears the count in X31Y68A and X31Y68B, blocking the assertion of INI/.

POC/ (Power On Clear) drives the Preset (pin 10) input of X31Y60B. This causes INI/ to be asserted during power-up, ensuring the Write Data FIFOs are initially reset.

**Modify Data and Mask Latch**

The BP bus multiplexer is shown on sheet 7 of the schematics. It consists of the two cascaded 4-bit data selectors located at X17Y73 and X14Y73, the octal D-type latch located at X12Y71 and the tri-state buffer located at X10Y71. All multiplexer components are driven by the DAT bus. The data selectors use DAT0-DAT7 or DAT8-DATF to drive BP0-BP7; the latch and buffer use DAT0-DAT7 or DAT8-DATF to drive BP8-BPF. The data selectors are the Modify Data portion of the Modify Data and Mask Latch block in Figure 21. The latch forms the Mask Latch portion of the Modify Data and Mask Latch block in Figure 21. The buffer drives BP8-BPF with DAT8-DATF in Modes 0 and 1.
NAND gate X6Y11B selects DAT0-DAT7 to drive BP0-BP7 if neither DBS/ (Double Byte Select) nor UBS/ (Upper Byte Select) is asserted. UBS/, an output of PAL B2 shown on sheet 4, is asserted when the PS/2 sends data on the upper half of the PS/2 to the Dataram data bus (PCD8-PCD15) in Modes 2 or 3. That is, UBS/ is asserted when writing single bytes to odd addresses in Modes 2 or 3. Therefore, in Modes 2 or 3, BP0-BP7 are driven by DAT0-DAT7 when writing to even addresses; they are driven by DAT8-DATF when writing to odd addresses.

DBS/, an output of PAL B5 shown on sheet 4, is asserted when the PS/2 sends data to the A Board using the upper half of the PS/2 to Dataram data bus (PCD8-PCD15). For more information on DBS/, refer to the A Board Data FIFOs section of the Data Bus Interface.

When the PS/2 writes to port 33CH, CMW (Change Mask Write) is asserted, latching DAT0-DAT7 into X12Y71 and DAT8-DATB into X8Y74. DAT0-DAT7 drive BP8-BPF via X12Y71 during Modes 2 or 3 because MC1 is high and its complement (unlabeled output of X8Y74's pin 11) is low. DAT8-DATF drive BP8-BPF during Modes 0 and 2 because MC1 is low, enabling X10Y71, and MC1's complement is high, disabling X12Y71. For BP bus operation during PS/2 to A Board transfers, refer to the Data Bus Interface (A Board Data FIFOs) description. Table 33 below summarizes BP bus data as a function of B Board Mode and address.

<table>
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<tr>
<th>Mode (Address)</th>
<th>UBS/</th>
<th>DBS/</th>
<th>BP0-BP7</th>
<th>BP8-BP15</th>
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<tr>
<td>0 (even)</td>
<td>1</td>
<td>1</td>
<td>DAT0-DAT7</td>
<td>DAT8-DATF</td>
</tr>
<tr>
<td>0 (odd)</td>
<td>0</td>
<td>1</td>
<td>DAT8-DATF</td>
<td>DAT8-DATF</td>
</tr>
<tr>
<td>0 (even)</td>
<td>1</td>
<td>1</td>
<td>DAT0-DAT7</td>
<td>DAT8-DATF</td>
</tr>
<tr>
<td>1 (odd)</td>
<td>0</td>
<td>1</td>
<td>DAT8-DATF</td>
<td>DAT8-DATF</td>
</tr>
<tr>
<td>2 (even)</td>
<td>1</td>
<td>1</td>
<td>DAT0-DAT7</td>
<td>Mask</td>
</tr>
<tr>
<td>2 (odd)</td>
<td>0</td>
<td>1</td>
<td>DAT8-DATF</td>
<td>Mask</td>
</tr>
<tr>
<td>3 (even)</td>
<td>1</td>
<td>1</td>
<td>DAT0-DAT7</td>
<td>Mask</td>
</tr>
<tr>
<td>3 (odd)</td>
<td>0</td>
<td>1</td>
<td>DAT8-DATF</td>
<td>Mask</td>
</tr>
</tbody>
</table>

Table 33. DB Bus Operation During Dataram Read/Write
Bus Flippers

The Bus Flippers consist of all PALs on sheets 13 through 16 of the schematics. Each PAL shown on these sheets operates on four data bits. Therefore, 32 PALs are required to handle the 128-bit data words.

The Bus Flippers block in Figure 21 is the functional equivalent of one bit section of each PAL. Thus, each PAL consists of four identical functional blocks. Each line connected to the Bus Flippers block on Figure 21 has either one or four numbers in parentheses. These are PAL pin numbers. A single number means the line is internally routed to each bit’s logic block. Four numbers mean the order listed is LSB to MSB, respectively, for the bits processed by that chip. For example, PAL X2Y116, shown on sheet 13, handles bits D001, D081, D161 and D241. Pin 13 is WD161, pin 15 is W161 and pin 4 is D161.

Refer to sheet 13 of the schematics. Note that there are two columns of chips. The four PALs making up the left column process these 16 data bits: D000, D080, D160, D240, D320, D400, D480, D560, D001, D081, D161, D241, D321, D401, D481 and D561. These bits are the 0 bits for bytes 0-15 and are referred to as bit plane 0. The same data bit and mask bit are applied to each chip (D000 and D080, respectively). The right column of PALs handles all bit plane 1 bits. The remaining 3 sheets of Bus Flipper schematics process bit planes 2 and 3, 4 and 5, and 6 and 7, respectively. Refer to the Bus Flippers description on page 6-30 for additional information.
Readback RAM Section

The Readback RAM section consists of the Readback RAM, Readback Address Multiplexer and the Readback Word Selector.

Readback RAM

The Readback RAM is shown on sheets 17 through 20 of the schematics. It consists of 32, 4-bit by 4096-word static RAMs that are cascaded to function as a 4096 by 128-bit RAM. These RAMs are dual ported. The D-inputs are driven by the W000-W631 outputs of the Bus Flippers; the Y-outputs drive R00-R7F, the Readback Word Selector’s input bus.

Data is written into the RAMs when RWS/ is low. RWS/, an output of PAL B6 shown on sheet 4, goes low during Mode 1 while WDTAC/ is asserted.

The A0-A11 address input lines of the Readback RAM are driven by the Readback Address Multiplexer’s RA0-RAB (Readback Address bits 0-B) bus. RA0-RAB are driven by the WIDE WORD Address Generator/Latch when data is being stored in the RAM; RA0-RAB are driven by the PS/2 via ADR4-ADRF when data is being read from the RAM.

Readback Address Multiplexer

The Readback Address Multiplexer is shown on sheet 3 of the schematics. It consists of the 3 cascaded 4-bit data selectors located at X14Y110, X12Y110 and X10Y110. Together, the selectors function as a 12-bit data selector. The A-inputs are driven by BAT0-BATB; the B-inputs are driven by ADR4-ADRF. The A-inputs are selected when RWA/ (Read/Write Address) is low; the B-inputs are selected when RWA/ is high. RWA/ is low while the B Board has control of the Dataram memory. Thus, while the B Board is reading the requested data from the Dataram memory and storing it in the Readback RAM, RWA/ is low. While the A Board is performing its raster read, RWA/ is high. During this time, providing the Readback cycle has completed as indicated by the Status Port, the PS/2 can read data from the Readback RAM.
Readback Word Selector

The Readback Word Selector is shown on sheets 21 and 22 of the schematics. It consists of 16 cascaded 8-lines to 1-line data selectors. Together, these selectors function as a 128- to 8-line or 128- to 16-line data selector. The selectors' data inputs are driven by the Readback RAM's output data bus (R00-R7F).

Data selection is accomplished by ADR1-ADR3 and RR0/-RR1/. Since the 4 LSBs of the address bus (ADR0-ADR3) are not used for WIDE WORD addressing by the Readback RAM, these bits are available for use as a byte address. However, since the PS/2 has the option of reading 8- or 16-bit words, only ADR1-ADR3 are used to address one of eight 16-bit words. The lower byte, upper byte or both bytes of this selected 16-bit word may be enabled onto the DAT bus by controlling the selectors' tri-state enable inputs.

The selectors shown on sheet 21 drive the lower half of the DAT bus (DAT0-DAT7) when RR0/ goes low. The selectors shown on sheet 22 drive the upper half of the DAT bus (DAT8-DATF) when RR1/ is low. When both RR0/ and RR1/ are low, both halves of the DAT bus are driven by the Readback Word Selector. RR0/ and RR1/ are outputs of PAL B3, a part of the Memory and I/O Mapped Control Decoder. For more information on RR0/ and RR1/, refer to the PAL B3 equations in the Reference section of this manual.
## Diagnostics

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McIDAS-OS2 WWW Diagnostics

The Diagnostics diskette contains the Level 1 and Level 2 diagnostics for the WIDE WORD Workstation (WWW).

Level 1 refers to Low Level Diagnostics which run outside the McIDAS-OS2 environment and allow you to manipulate the WWW at the register, word and bit levels of its domain. Level 2 refers to High Level Diagnostics which run inside the McIDAS-OS2 environment and allow you to manipulate the WWW with a few simple keystrokes.

Installing Level 1 Diagnostics

Use the instructions below to install the Level 1 diagnostics.

1. Switch to the drive or partition on which the McIDAS\TOOLS\ and McIDAS\CODE directories reside, usually the C: drive.

2. Make sure the WWW Diagnostics diskette is in the A: drive. Then,

   Type: A:INSTALL1
   Press: Enter

   This will unarchive the files you need to run Level 1 diagnostics, placing the executable programs and .PIC files in the tools directory, and appropriate menus and help files in the data directory (McIDAS\DATA).

3. Use an optional drive argument if the McIDAS code and data reside on different drives or partitions on your PS/2. For example,

   Type: A:INSTALL1 D:
   Press: Enter

   if you put the MCIDAS\DATA directory on the D: drive when you installed McIDAS-OS2.

4. For instructions on how to run and use Level 1 diagnostics, refer to C:\MCIDAS\TOOLS\LLDIAGS.DOC or its printed counterpart.
Installing Level 2 Diagnostics

Use the instructions below to install the Level 2 diagnostics.

1. Switch to the drive or partition on which the McIDAS\TOOLS and McIDAS\CODE directories reside (usually the C: drive).

2. Make sure the WWW Diagnostics diskette is in the A: drive. Then,
   - Type: A:INSTALL2
   - Press: Enter

   This entry will unarchive the files you need to run Level 2 diagnostics, placing the executable programs in the code directory, and the LW files and areas in the data directory. If you are using the Menu system, your existing menu file (MENU) will be renamed MENU.BAK. You must copy MENU.BAK back into MENU when you finish running Level 2 diagnostics.

3. Use an optional drive argument if the McIDAS code and data reside on different drives or partitions on your PS/2. For example,
   - Type: A:INSTALL2 D:
   - Press: Enter

   if you put the MCIDAS\DATA directory on the D: drive when you installed McIDAS-OS2.

4. Switch back to your McIDAS-OS2 session. Then enter the command below to run the Level 2 diagnostics.
   - Type: DIAGS MENU=INSTALL
   - Press: Enter

   This installs the diagnostics menu.

5. To invoke the diagnostics menu,
   - Press: Esc

   Then follow the menu selections. The F12 key exits this menu.
6. When you're finished running Level 2 diagnostics,

Type: DIAGS MENU=REMOVE
Press: Enter

to deactivate the diagnostics menu.

DIAGS is a local McIDAS-OS2 command that is listed in the command list generated by typing HELP. To obtain the correct syntax for running DIAGS,

Type: HELP DIAGS
Press: Enter
Using McIDAS-OS2 Low Level Diagnostics

Low Level Diagnostics are software diagnostic tests/tools designed to run outside the McIDAS-OS2 environment and allow you to manipulate the WWW at the register, word and bit levels of its domain.

Currently, the Low Level Diagnostic utility is a menu driven set of programs. They are presented in the main diagnostic menu as follows:

- WWW series of diagnostics
- SDXS diagnostics
- Low Level utilities

WWW Diagnostics
The WWW series of diagnostics performs such tasks as:

- line write (256-level gray scale) on line 1 of the image
- line write (alternating B&W blocks of pixels) on line 1 of the image
- read segment test, which performs a read of segment 0 at TV rates on a continuous basis
- write/read check, which performs a write of segment 0, then reads it back from the WWW and displays the results on the screen
- loading a repeating gray scale into a frame
- generating two 100x100 cursors (1 red crosshair, 1 cyan box)
- loading a gray scale and 2 cursors
- performing a fast erase of frame 0

SDXS Diagnostics
The SDXS diagnostics allow writing to any WWW I/O port or control word, or writing any word to image memory. This can be done once, or repeatedly at TV rates, or as fast as possible.

Low Level Utilities
Low Level utilities:

- read WWW input port 33Ch and report findings (WIDE WORD memory size, command/data FIFO information)
- read WWW input port 33Eh and reporting findings (FIFO/Address/Data overflows, Readback RAM flag)
- erase lines/frames quickly (prompts for frame and erase information)
- set frame pointer and channel information for viewing that frame
set start addresses for all channels (0/1/2) either to the same or different values
set the zoom value for all channels (0/1/2) either to the same or different values
set the Channel Mask for a specific channel (0/1/2 or Dual Channel)
set the Display Mode, Horizontal/Vertical switch line/pixel, etc.

Other Low Level Utilities:
prompt for frame information and save the picture displayed on a given frame into a .PIC file which can later be restored to the WWW
prompt for file and frame information, and restore a .PIC file to a specified frame
connect cursor 2 to the mouse driver; the mouse can then be moved and used to determine the position of the cursor in a frame
  - mouse button 1 changes the cursor size
  - mouse button 2 reports TV line and element
  - mouse buttons 1 and 2 together disengage cursor 2 from the mouse
invoke a utility to examine the contents of the WWW Shadow Segment; can be used to examine individual values or dump the entire segment
generate a quad-panel display of the Channel 1 VIS image and Channel 2 IR image with labeling, blinking, window cursor, and nortle

Running LLDIAGS

Use the steps below to run the Low Level Diagnostics program.

1. Exit McIDAS by entering the McIDAS-OS2 command EXIT.
   Type: EXIT
   Press: Enter

2. Switch to another * OS/2 session *.
   Press: Alt + Esc (simultaneously)
3. Make sure you are in the \MCIDAS\TOOLS directory.

   Type: CD\MCIDAS\TOOLS
   Press: Enter

4. Type: LLDIAGS
   Press: Enter

5. You can now exercise the diagnostics. The menus and HELP will help you perform the tests. Use F10 to exit a menu level, including the main menu level which gets you out of LLDIAGS entirely. Use F12 to display the HELP for a given menu level.

Shadowing

Except for two minor exceptions, you cannot ask the WIDE WORD to tell you what its current state is, i.e., report the contents of control registers, enhancement tables, etc. The two exceptions are input ports 33Ch and 33Eh which can be interrogated/examined by Utilities, CheckC and CheckE.

Although you can’t ask the WWW to ascertain its current state, the WWW has a shadowing scheme that keeps a copy (shadow) of all control information sent to it. The LLDIAGS program, when invoked, allocates a shared memory segment. All subsequent LLDIAGS activity with the WWW is then shadowed in this shared memory segment.

Most Low Level Diagnostic utilities look in this shadow to retrieve and report prior settings. Sometimes the reported prior setting may look like garbage. No matter what the reported old shadow settings/values are, the new values generated by a given utility and sent to the WIDE WORD are different and correct. Furthermore, all subsequent peeks into the shadow will reflect past activity correctly.

In short, it sometimes occurs that initial shadow values may not be correct but are not harmful and do get corrected. Running SDXS (item 2 in the Main Menu) clears/initializes all shadow values to zero and initializes the WWW (enhancements, cursors, etc.).
Clearing the WWW

If you cannot clear the WWW by running SDXS, or if you want to be sure of the current state of the WWW for diagnostic/testing purposes, you can clear it by powering down, waiting 10 seconds, and powering up again. Then run SDXS (item 2 of the Main Menu) to initialize the WWW. When SDXS asks if you want to initialize the WWW, respond appropriately.

Allocating Frames, Frame Numbers and Channels in McIDAS-OS2

If you use the WWW diagnostics in conjunction with images/graphics loaded into the WWW by McIDAS-OS2, note that McIDAS-OS2 allocates frames which are usually 640x480 pixels. It uses Channel 0 to display graphics and Channel 1 to display images. McIDAS-OS2 refers to Image Frame 1, 2, 3, etc., when dealing with images, and Graphics Frame 1, 2, 3, etc., when dealing with graphics. McIDAS-OS2 allocates frames in this order: ImgFrm1, GrphFrm1, ImgFrm2, GrphFrm2, etc.

Low Level Diagnostics don’t distinguish between image and graphics frames, and simply refer to generic frames starting at 0, and increasing by 1. For example, if you load images into frames 1 and 2 in McIDAS-OS2, draw corresponding MAPs in graphics frames 1 and 2, then exit McIDAS-OS2 and want to view the individual "frames" currently held by the WWW, image1 will be in frame 0, graphics1 will be in frame 1, image2 will be in frame 2, and graphics2 will be in frame 3 (from the Low Level Diagnostics point of view).

SDXS and a few other Low Level Diagnostics load a 1024x512 image into frame zero for diagnostic purposes.

Verifying the Enhancement Table

Figure 23 on the next page shows the bit codes corresponding to the enhancement tables. To verify the enhancement tables, compare the color plate behind this page with your screen. Variation from these color patterns indicates certain bits in the enhancement tables are incorrect or are being used incorrectly.
Figure 23. Bit Codes for Enhancement Table Verification
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A Board PAL Equations

Declarations

Declarations list the logic conventions and format for the signal names. The signal names are in uppercase letters and numbers.

The first group of signal names refers to the power and ground rails. The second group refers to the input signals received by the device. The third group refers to the outputs from the PAL. The respective pin numbers that make each of these connections are given in the line below the signal names.

Equations

The logic equations that generate each signal are shown in their highest order form using the symbols and abbreviations described below.

Symbols and Abbreviations

The following is an example of a PAL equation.

\[ \neg\text{NCS} = \text{ncs} \& \neg\text{G} \]
\[ \# \text{ncs} \& \neg\text{F} \]
\[ \# \text{ncs} \& \neg\text{E} \]
\[ \# \text{ncs} \& \neg\text{D} \]
\[ \# \text{OEL} \& ((\text{Address}>=^\text{h800}) \& (\text{Address}<=^\text{h876})) \]

Below is an explanation of the symbols and abbreviations used in the equation.

<table>
<thead>
<tr>
<th>Symbol/Abbreviation</th>
<th>Explanation</th>
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<tbody>
<tr>
<td>!</td>
<td>the one's complement of, e.g. ( \neg\text{NCS} = \overline{\text{NCS}} )</td>
</tr>
<tr>
<td>:</td>
<td>a register latched signal; valid on the rising edge of the register clock</td>
</tr>
<tr>
<td>&amp;</td>
<td>Logical AND</td>
</tr>
<tr>
<td>#</td>
<td>Logical OR</td>
</tr>
<tr>
<td>ncs</td>
<td>combined terms qualify the ncs mode*</td>
</tr>
<tr>
<td>Address&lt;=^h876</td>
<td>combined terms are less than or equal to h876 hexadecimal*</td>
</tr>
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*Terms combined to form address values and ncs, etc., are listed in the Equations section in the Address = or ncs = line.
Refresh Control PAL A1

Device Location
X45Y1

Device Type
P16L8

Module
WWA1, flag r1

Revision Date
10/26/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 10, 20

HQA, HQB, HQC, HQD, HQE, HQF, HCR, RRE, VG
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

CBF, VI, OEF, HQG, FI, RRS, REF, HRG, WREN
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Address=[X, HQG, HQF, HQE, HQD, HQC, HQB, HQA]

Equations
enable WREN = TRUE

!WREN = !HRG & RRE & CBF

enable HRG = TRUE

!HRG = HCR & !HRG
# (Address==^h46)

enable REF = TRUE

!REF = HRG & ((Address>=^h14) & (Address<=^h37))
# HRG & ((Address>=^h38) & (Address<=^h3B))

enable RRS = TRUE

!RRS = HRG & VG & (Address==^h45)

enable VI = TRUE
\[ \text{!VI} = \text{!VG} \]

\[ \text{enable FI} = \text{TRUE} \]

\[ \text{!FI} = \text{!VG} \& \text{!OEF} \]
Vertical Decode PAL A2A

Device Location
X43Y12

Device Type
P22V10A

Module
WWA2A, flag r1

Revision Date
07/10/91

Declarations
TRUE, FALSE = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 12, 24

A, B, C, D, E, F, G, H, I, J, NC
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

OEF, VCR, VI0, VI1, VI2, OFP, VG, VI, DVG, DVI, LSL
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = [X, X, J, I, H, G, F, E, D, C, B, A]

Equations

VI0 = (Address >= ^h000) & (Address <= ^h005)
# (Address >= ^h00C) & (Address <= ^h011)
# (Address == ^h2C)

VI1 = (Address >= ^h000) & (Address <= ^h005)
# (Address >= ^h00C) & (Address <= ^h02B)

VI2 = (Address >= ^h006) & (Address <= ^h00B)

!VG = (Address >= ^h000) & (Address <= ^h02B)

!VI = (Address >= ^h000) & (Address <= ^h02B)

!DVG = (Address >= ^h000) & (Address <= ^h02C)

DVI = (Address >= ^h000) & (Address <= ^h02C)

!LSL_ = (Address == ^h204)

!VCR = (Address == ^h20C)

!OFP = OEF & (Address == ^h20C)
Horizontal Decode PAL A3

Device Location  X43Y47

Device Type  P22V10A

Module  WWA3, flag r1

Revision Date  06/05/89

Declarations  TRUE, FALSE = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 12, 24

A, B, C, D, E, F, G, H, I, J, VI0
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

VI1, VI2, OEL, HCR, NBF, NCB, NCS, BLANK, SYNC, DLG, LG
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = [X, X, X, VI2, VI1, VI0, J, I, H, G, F, E, D, C, B, A]

ncs = (OEL & !VI1 & !VI2 & !H & !I & !J)

Equations

LG = ((Address >= ^h0000) & (Address <= ^h007F))
# ((Address >= ^h0300) & (Address <= ^h03FF))
# ((Address >= ^h0400) & (Address <= ^h047F))
# ((Address >= ^h0700) & (Address <= ^h07FF))
# VI1
# VI2
#DV1

DLG = ((Address >= ^h0000) & (Address <= ^h007F))
# ((Address >= ^h0300) & (Address <= ^h03FF))
# VI0
# VI1
# VI2
#DV1

!SYNC := !F & !G & !H & !I & !J "0-33 ALL LINES
# J & !I & H & G & F & !E & D "745+ ALL LINES
# J & !I & H & G & F & E
# J & I
# ((Address >= ^h1000) & (Address <= ^h1292))
!BLANK = ((Address >= ^h000) & (Address <= ^h0082))
# ((Address >= ^h0302) & (Address <= ^h03FF))
# VI0
# VI1
# VI2
# DV1

!HCR = A & B & D & I & J

"PIXEL 780"

!NCS = ncs & !G
# ncs & !F
# ncs & !E
# ncs & !D
# OEL & ((Address >= ^h800) & (Address <= ^h876))

# ((Address >= ^h0C00) & (Address <= ^h0C3F))

# ((Address = ^h1000) & (Address <= ^h129B))

!NCB = OEL & ((Address >= ^h0000) & (Address <= ^h00EE))
# !OEL & ((Address >= ^h02E3) & (Address <= ^h03FF))
# VI0
# VI1
# VI2

DV1: = VI1
Parameter Address PAL A4

Device Location
X57Y23

Device Type
P22V10A

Module
WWA4, flag r1

Revision Date
02/27/88

Declarations
TRUE, FALSE = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 12, 24

STB, A11, A10, AF, AE, AD, AC, AB, AA, A9, A8
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

NC, WEDC, WEI2, WEI1, WEGC, CLD, LSA, USA, LLL, ZFL, CL0
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = [X, X, A11, A10, AF, AE, AD, AC, AB, AA, A9, A8]

Equations
!CL0 = STB & ((Address>=^h200) & (Address<=^h2FF))
!ZFL = STB & ((Address>=^h018) & (Address<=^h01D))
!LLL = STB & ((Address>=^h010) & (Address<=^h015))
!USA = STB & ((Address>=^h008) & (Address<=^h00D))
!LSA = STB & ((Address>=^h000) & (Address<=^h005))
!CLD = STB & ((Address>=^h040) & (Address<=^h05F))
!WEGC = STB & ((Address>=^h090) & (Address<=^h09F))
!WEI1 = STB & ((Address>=^h0C0) & (Address<=^h0CF))
!WEI2 = STB & ((Address>=^h0F0) & (Address<=^h0FF))
!WEDC = STB & ((Address>=^h100) & (Address<=^h1FF))
Parameter Address PAL A5

Device Location  X53Y12
Device Type      P22V10A
Module            WWA5, flag r1
Revision Date     10/27/88

Declarations
TRUE, FALSE = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin  12, 24

STB, A11, A10, AF, AE, AD, AC, AB, AA, A9, A8
pin  1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

NC, MI2, MI1, MGC, MDC, BRL, CLL, PMSL, PVSL, PHSL, CL1
pin  13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = [X, X, A11, A10, AF, AE, AD, AC, AB, AA, A9, A8]

Equations
!CL1 = STB & ((Address>=^h300) & (Address<=^h3FF))

!PHSL = STB & (Address==^h007)

!PVSL = STB & (Address==^h006)

!PMSL = STB & (Address==^h00E)

!CLL = STB & (Address==^h020)

!BRL = STB & (Address==^h00F)

!MDC = STB & (Address==^h01F)

!MGC = STB & (Address==^h016)

!MI1 = STB & (Address==^h017)

!MI2 = STB & (Address==^h01E)
Parameter Address PAL A6

Device Location  X53Y25
Device Type      P22V10A
Module           WWA6, flag r1
Revision Date    10/27/88

Declarations
TRUE, FALSE = 1, 0
X, Z, Ck = .X., .Z., .C.
GND, VCC
pin 12, 24

STB, A11, A10, AF, AE, AD, AC, AB, AA, A9, A8
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

NC, C1T, C1VS, C1VP, C1HS, C1HP, C0T, C0VS, C0VP, C0HS, C0HP
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = [X, X, A11, A10, AF, AE, AD, AC, AB, AA, A9, A8]

Equations
!C0HP = STB & (Address==^h021)
!C0HS = STB & (Address==^h023)
!C0VP = STB & (Address==^h022)
!C0VS = STB & (Address==^h024)
!C0T  = STB & (Address==^h025)
!C1HP = STB & (Address==^h026)
!C1HS = STB & (Address==^h028)
!C1VP = STB & (Address==^h027)
!C1VS = STB & (Address==^h029)
!C1T  = STB & (Address==^h02A)
Cursor Size PAL A7

Device Location  
X31Y7, X28Y5

Device Type  
P22V10A

Module  
WWA7, flag r1

Revision Date  
11/22/88

Declarations  
TRUE, FALSE = 1, 0  
X, Z, Ck = .X., .Z., .C.

GND, VCC  
pin 12, 24

HRC, HQA, HQB, HQC, MCB, VRC, VQA, VQB, VQC, CT0, CT1  
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

CT2, VCE, WCC, CC, SWC, SBC, BCH, CHC, BOX, OFF, HCE  
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations  
ulp = (IHRC & HQC & ! HQB & ! HQA & ! VRC & VQC & ! VQB & ! VQA)

ult = (IHQC & HQB & ! VRC & VQC & ! VQB & ! VQA)

utc = (IHRC & ! HQC & HQB & HQA & ! VRC & VQC & ! VQB & ! VQA)

vlr = (IHRC & HQC & ! HQB & ! HQA & ! VQC & VQB)

vcl = (IHRC & ! HQC & HQB & HQA &! VQC & VQB)

vrs = (IHRC & ! HQC & HQB & ! HQA & ! VQC & VQB)

lcp = (IHRC & HQC & ! HQB & ! HQA & ! VRC & ! VQC & VQB & VQA)

hcl = (IHQC & HQB & ! VRC & ! VQC & VQB & VQA)

cp = (IHRC & ! HQC & HQB & HQA & ! VRC & ! VQC & VQB & VQA)

bl = (IHQC & HQB & ! VRC & ! VQC & VQB & ! VQA)

sb = (IHQC & HQB & ! VQC & VQB)

tc = (IHRC & IHQC & HQB & HQA & VQC)
bcl = (!HRC & !HQC & HQB & HQA & !VQC & !VQB)

lcl = (HQC & !VRC & !VQC & VQB & VQA)

rcl = (IHQC & !HQB & !VRC & !VQC & VQB & VQA)

!HCE = HQC
  # HQB

enable OFF = !CT0 & !CT1 & !CT2

OFF = FALSE

enable BOX = CT0 & !CT1 & !CT2

BOX = ulp
  # utl
  # vls
  # vrs
  # bl

enable CHC = !CT0 & CT1 & !CT2

CHC = utc
  # vcl
  # lcp
  # hcl

enable BCH = CT0 & CT1 & !CT2

BCH = ulp
  # utl
  # vls
  # vrs
  # bl
  # vcl
  # hcl

enable SBC = !CT0 & !CT1 & CT2

SBC = ulp
  # utl
  # vls
  # sb

enable SWC = CT0 & !CT1 & CT2
SWC = ulp
# utl
# vls
# vrs
# bl
# cp
# tcl
# bcl
# lcl
# rcl

enable CC = !CT0 & CT1 & CT2

CC = sb & MCB

enable WCC = CT0 & CT1 & CT2

!WCC = sb & MCB

!VCE = VQC
# VQB
Cursor Type PAL A8

Device Location
X33Y21, X31Y20

Device Type
P16L8

Module
WWA8, flag r0

Revision Date
10/27/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0

GND, VCC
pin 10, 20

VRC, HQA, VQC, VG, VCR, VQA, VQB, FD0, FD1
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

FD2, VCL, A7, CTL4, CT0, CT1, CT2, AI5, NC
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Equations
enable AI5 = !VG

!AI5 = !VQA

enable CT2 = TRUE

!CT2 = CTL & !CT2
# !CTL & !FD2

enable CT1 = TRUE

!CT1 = CTL & !CT1
# !CTL & !FD1

enable CT0 = TRUE

!CT0 = CTL & !CT0
# !CTL & !FD0

enable A7 = !VG

!A7 = !HQA
enable VCL = TRUE

!VCL = !VCR
# !VRC & !VQC
# !VRC & VQC & !VQB & !VQA
Vertical Switch PAL A9

Device Location  X43Y93
Device Type  P22V10A
Module  WWA9, flag r1
Revision Date  12/02/88

Declarations
TRUE, FALSE = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 12, 24

LG, VG, VRC, G, LD8, LD9, LDA, LDB, LDC, LDD, LDE
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

OEF, TBG, HSE, MC0, MC1, W, HSL, DTB, QG, LRS, VSG
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations
!VSG = !QG & LDC

QG := !VG & G
# VG & VRC & QG
# VG & !VRC & !QG

"LOAD
"HOLD
"COUNT

DTB = TBG & LDC
# !VRC & !QG & LDC

!HSL = !VRC & !QG & LDC

W = LDB & !LDC & !LDD & !LDE
# !TBG & LDB & LDC & !LDD & !LDE
# TBG & LD9 & LDC & !LDD & !LDE
# !LRS & LDB & !LDC & LDD & !LDE
# LRS & LDA & !LDC & LDD & !LDE
# !LRS & !TBG & LDB & LDC & LDD & !LDE
# LRS & !TBG & LDA & LDC & LDD & !LDE
# !LRS & !TBG & LD9 & LDC & LDD & !LDE
# LRS & !TBG & LD8 & LDC & LDD & !LDE
# LDB & !LDC & LDE
# LDB & !TBG & LDE
# LD9 & !TBG & LDE

"FULL SCREEN
"VERT TOP
"VERT BOTTOM
"HORIZ LEFT
"HORIZ RIGHT
"QUAD TOP LEFT
"QUAD TOP RIGHT
"QUAD BOT LEFT
"QUAD BOT RIGHT
"FULL STEREO/3 WAY
"TOP STEREO/3 WAY
"BOT STEREO/3 WAY

Issued 3/91
MC1 = OEF & !LDD & LDE  
# LDD & LDE
MC0 = !OEF & !LDD & LDE  
# LDD & LDE
HSE = LRS & LDD & !LDE

TBG := !VRC & !QG  
# TBG & VG

"SET
"HOLD/RESET
Panel Channel PAL A10

Device Location  X41Y77
Device Type      P22V10A
Module           WWA10, flag r1
Revision Date    11/27/88

Declarations
   TRUE, FALSE = 1, 0
   X, Z, Ck = .X., .Z., .C.
   GND, VCC
      pin 12, 24
   CLK, PT0, PT1, PT2, PT3, PT4, PT5, PT6, PT7, HSE, TBG
      pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
   LDC, LCL, LVB, I2MA, I1MA, GMA, I2LB, I1LB, GLB, I2, I1
      pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations
   I1 := PT7 & !HSE & !LDC
      # PT7 & !HSE & !TBG
      # PT5 & HSE & ILDC
      # PT5 & HSE & !TBG
      # PT3 & !HSE & TBG & LDC
      # PT1 & HSE & TBG & LDC
   I2 := PT6 & !HSE & !LDC
      # PT6 & !HSE & !TBG
      # PT4 & HSE & !LDC
      # PT4 & HSE & !TBG
      # PT2 & !HSE & TBG & LDC
      # PT0 & HSE & TBG & LDC
   GLB = GMA & !LVB
      # GMA & !LCL
   I1LB = I1MA & !LVB
      # I1MA & !LCL
   I2LB = I2MA & !LVB
      # I2MA & !LCL

Issued 3/91
Prioritizer PAL A11

Device Location
X39Y101

Device Type
P22V10A

Module
WWA11, flag r1

Revision Date
11/21/88

Declarations
TRUE, FALSE = 1, 0

GND, VCC
pin 12, 24

UG, CB1, CB2, W, MS0, MS1, WC2, II1, II2, LBG, LB1
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

LG, LB2, LCG, SC1, GDE, DC1, DC2, DCE, SC2, CLD, CLI
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations
!CLI = MS1 & MS0

!CLD = !LCG & LBG & MS1 & MS0
# !CB1 & !W & !I1 & !I2 & !MS0 & !MS1
# !CB2 & !W & !I1 & !I2 & !MS0 & !MS1

SC2 = !UG & !MS1 & MS0
# !UG & MS1 & !MS0
# LBG & !MS1 & MS0
# LBG & MS1 & !MS0
# LB2 & !LCG

DCE = MS1
# MS0
# CB1
# CB2
# !WC2
# !LG & W
# !UG & W
# LBG
# !I1
# !I2
DC2 = MS0
# CB1 & !MS1 & !MS0
# CB2 & !MS1 & !MS0
# !LG & W & !MS1 & !MS0
# !UG & W & !MS0
# LBG
# !I1 & !I2 & WC2 & !MS1 & !MS0
# I1 & WC2 & !MS1 & !MS0

DC1 = MS1
# CB1 & !MS1 & !MS0
# CB2 & !MS1 & !MS0
# !WC2 & !MS1 & !MS0
# !LG & W & !MS1
# !UG & W & !MS1 & !MS0
# LBG
# I2 & !MS1 & !MS0
# !I1 & !I2 & !MS1 & !MS0

!GDE = !LG & W & !MS1
# !UG & W & !MS0
# CB1 & !MS1 & !MS0
# CB2 & !MS1 & !MS0
# LBG
# !I2 & !I1 & !MS1 & !MS0
# MS1 & MS0

SC1 = !LG & !MS1 & MS0
# !LG & MS1 & !MS0
# LBG & !MS1 & MS0
# LBG & MS1 & !MS0
# LB1 & !LCG
Channel Blanking Decoder PAL A12

Device Location
X23Y92

Device Type
P16L8A

Module
WWA12, flag r0

Revision Date
03/02/89

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0

GND, VCC
pin 10, 20

LRS, TBG, I1MC, I1MD, I1ME, I1MF, I2MC, I2MD, I2ME
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

I2MF, VB1, GMC, GMD, GME, GMF, GLB, VBG, VB2
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Equations
!VB2 = !TBG & I2MC
# TBG & I2MD
# !LRS & I2ME
# LRS & I2MF

!VBG = !TBG & GMC
# TBG & GMD
# !LRS & GME
# LRS & GMF
# GLB

!VB1 = !TBG & I1MC
# TBG & I1MD
# !LRS & I1ME
# LRS & I1MF
Address Range Control PAL A13

Device Location  X12Y53

Device Type  P16L8A

Module  WWA13, flag r0

Revision Date  05/02/89

Declarations  TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
   pin 10, 20

W4, W5, W6, W7, W8, W9, W10, M19, M1A
   pin 1, 2, 3, 4, 5, 6, 7, 8, 9

M1B, ARE, M1C, M1D, M1E, M1F, AOE
   pin 11, 12, 13, 14, 15, 16, 17

Equations  enable AOE = TRUE

!AOE = W4 & W5 & W6 & W7 & M19  "200 FRAMES
# W4 & !W5 & W6 & W7 & M19 & M1A  "300 FRAMES
# W5 & W6 & W7 & M1A  "400 FRAMES
# W6 & W7 & M1B  "800 FRAMES
# W6 & !W7 & M1B & M1C  "1200 FRAMES
# W7 & M1C  "1600 FRAMES

enable ARE = TRUE

!ARE = AOE & !M1D & !M1E & !M1F
B Board PAL Equations

PC Bus Decode PAL B1

Device Location  X31Y114
Device Type      P22V10A
Module           WWB1, flag r1
Revision Date    04/26/89
Declarations     TRUE, FALSE = 1, 0
                 X, Z, Ck = .X., .Z., .C
                 GND, VCC
                 pin 12, 24
                 LK, P16, PBH, PW, PR, PMW, PMR, SEL, RST
                 pin 1, 2, 3, 4, 5, 6, 7, 9, 10
                 DS, INIT, R DY, PRD, MR, MW, IOR, IOW, BHE, A10
                 pin 14, 15, 16, 17, 18, 19, 20, 21, 22, 23
Equations        A10 = P16
                 BHE = PBH
                 !IOW = !PW & DS
                 !IOR = !PR
                 # !IOR & DS
                 !MW = !PMW & DS
                 !MR = !PMR
                 # !MR & DS
                 !PRD = !PR
                 # !PMR
RDY = !PR
    # !PW
    # !PMR
    # !PMW

INIT := RST

DS = RDY
Load Decode PAL B2

Device Location  X35Y105
Device Type      P22V10A
Module           WWB2, flag r1
Revision Date    12/20/88
Declarations     TRUE, FALSE = 1, 0
                 X, Z, Ck = .X., .Z., .C
                 GND, VCC
                 pin 12, 24
                 A0, A1, A2, A3, A4, WLG, A10, BHE, MC0, MC1, MW
                 pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
                 WR, UBS, AL, L7, L6, L5, L4, L3, L2, L1, L0
                 pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23
                 write = (!MC0 & !MC1 & A10 & !MW & !WLG)
                 read = (MC0 & !MC1 & A10 & !MW)
                 byte = (MC1 & A10 & !MW)
                 erase = (MC0 & MC1 & A4 & !WR)
                 Address = [A8, A2, A1, X]
Equations

!L0 = write & (Address==^h0) & !A0
# read & !A0
# byte

!L1 = write & (Address==^h0) & !BHE
# read & !BHE
# byte

!L2 = write & (Address==^h2) & !A0
# read & !A0
# byte & !MC0
# erase & (Address==^h8) & !A0

!L3 = write & (Address==^h2) & !BHE
# read & !BHE
# byte & !MC0
# erase & (Address==^h8) & !BHE
!L4 = write & (Address==^h4) & !A0
# read & !A0
# byte & !MC0
# erase & (Address==^hA) & !A0

!L5 = write & (Address==^h4) & !BHE
# read & !BHE
# byte & !MC0
# erase & (Address==^hA) & !BHE

!L6 = write & (Address==^h6) & !A0
# read & !A0
# byte

!L7 = write & (Address==^h6) & !BHE
# read & !BHE
# byte

!AL = write & (Address==^hE) & !BHE
# read & !BHE
# byte

!UBS = byte & A0
Load Decode PAL B3

Device Location  X35Y92
Device Type      P22V10A
Module           WWB3, flag r1
Revision Date    12/20/88
Declarations     TRUE, FALSE = 1, 0
                  GND, VCC
                  pin  12, 24
                  A0, A1, A2, A3, A10, BHE, MC0, MC1, MW, MR, WL
                  pin  1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
                  IOW, RR1, RR0, ALC, LE, LD, LC, LB, LA, L9, L8
                  pin  13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23
write = (!MC0 & !MC1 & A10 & !MW & !WL)
read  = (MC0 & !MC1 & A10 & !MW)
byte  = (MC1 & A10 & !MW)
Address = [A3, A2, A1, X]

Equations

%!L8 = write & (Address==^h8) & !A0
# read & !A0
# byte

%!L9 = write & (Address==^h8) & !BHE
# read & !BHE
# byte

%!LA = write & (Address==^hA) & !A0
# read & !A0
# byte

%!LB = write & (Address==^hA) & !BHE
# read & !BHE
# byte

%!LC = write & (Address==^hC) & !A0
# read & !A0
# byte
!LD = write & (Address==^hC) & !BHE
  # read & !BHE
  # byte

!LE = write & (Address==^hE) & !A0
  # read & !A0
  # byte

!ALC = !MW & A10

!RR0 = A10 & !A0 & !MR

!RR1 = A10 & !BHE & !MR
Load Decode PAL B4

Device Location  X10Y93
Device Type      P22V10A
Module           WWB4, flag r1
Revision Date    10/02/88

Declarations
TRUE, FALSE = 1, 0

GND, VCC
pin 12, 24

A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, AA
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

AB, BHE, RD, WR, MSL, STAT, MS1Z, CMW, UAW
pin 13, 14, 15, 16, 19, 20, 21, 22, 23

Address=[X, WR, RD, BHE, AB, AA, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0]

Equations
!UAW = (Address==^h233E)
!CMW = (Address==^h233C)
!MS1Z = (Address==^h433C)
!STAT = (Address==^h433E)
!MSL = (Address==^h2336)
# (Address==^h3336)
Command FIFO Load PAL B5

Device Location
X20Y46

Device Type
P22V10A

Module
WWB5, flag r1

Revision Date
11/23/88

Declarations
TRUE, FALSE = 1, 0

GND, VCC
pin 12, 24

MW, A0, BH, S0, S1, S2, S3, A10, AF, AE, AD
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

AC, L0, L1, L2, L3, L4, L5, AL, DB, AD11, AD10
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = [X, X, X, A10, S3, S2, S1, S0, AF, AE, AD, AC]

Equations
AD10 = ((Address>=^h010) & (Address<=^h03F))
# ((Address>=^h050) & (Address<=^h05F))

AD11 = ((Address>=^h040) & (Address<=^h05F));!DB = !BH &
((Address>=^h000) & (Address<=^h003))

!AL = !MW & !BH & ((Address>=^h000) & (Address<=^h006))
# !MW & !BH & (Address>=^h009)
# !MW & !BH & (Address>=^h00C)
# !MW & !BH & (Address>=^h00F)
# !MW & !BH & ((Address>=^h030) & (Address<=^h05F))

!L5 = !MW & !BH & ((Address>=^h004) & (Address<=^h006))
# !MW & !BH & (Address>=^h009)
# !MW & !BH & (Address>=^h00C)
# !MW & !BH & (Address>=^h00F)
# !MW & !BH & ((Address>=^h030) & (Address<=^h05F))
!L4 = !MW & !A0 & ((Address>=^h000) & (Address<=^h006))
# !MW & !A0 & (Address>=^h009)
# !MW & !A0 & (Address>=^h00C)
# !MW & !A0 & (Address>=^h00F)
# !MW & !A0 & ((Address>=^h030) & (Address<=^h05F))

!L3 = !MW & !BH & ((Address>=^h004) & (Address<=^h006))
# !MW & !BH & (Address>=^h008)
# !MW & !BH & (Address>=^h00B)
# !MW & !BH & (Address>=^h00E)
# !MW & !BH & ((Address>=^h020) & (Address<=^h02F))
# !MW & !BH & ((Address>=^h040) & (Address<=^h05F))

!L2 = !MW & !BH & ((Address>=^h000) & (Address<=^h003))
# !MW & !A0 & ((Address>=^h004) & (Address<=^h006))
# !MW & !A0 & (Address>=^h008)
# !MW & !A0 & (Address>=^h00B)
# !MW & !A0 & (Address>=^h00E)
# !MW & !A0 & ((Address>=^h020) & (Address<=^h02F))
# !MW & !A0 & ((Address>=^h040) & (Address<=^h05F))

!L1 = !MW & !BH & ((Address>=^h004) & (Address<=^h007))
# !MW & !BH & (Address>=^h00A)
# !MW & !BH & (Address>=^h00D)
# !MW & !BH & ((Address>=^h010) & (Address<=^h01F))
# !MW & !BH & ((Address>=^h040) & (Address<=^h05F))

!L0 = !MW & !A0 & ((Address>=^h000) & (Address<=^h007))
# !MW & !A0 & (Address>=^h00A)
# !MW & !A0 & (Address>=^h00D)
# !MW & !A0 & ((Address>=^h010) & (Address<=^h01F))
# !MW & !A0 & ((Address>=^h040) & (Address<=^h05F))
Read/Write Control PAL B6

Device Location  X8Y23
Device Type      P16R4A
Module           WWB6, flag r0
Revision Date    10/12/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C

GND, VCC
pin 10, 20

CLK, DR1, DR2, VI, UBF, WRD, MC1, WDC, WLO
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

OE, RWS, RCK, HPC, A0, UFR, LFR, WTG, DLS
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Equations
enable DLS = TRUE

!DLS = !HPC
# LFR & UFR

enable WTG = TRUE

!WTG = WRD & WLO

!LFR := !HPC & !LFR
# HPC & LFR & DR1 & DR2 & !VI

!UFR := !HPC & !UFR
# HPC & !LFR & UBF

!A0 := HPC & !A0
# !HPC & UFR

!HPC := HPC

enable RCK = TRUE

Issued 3/91
!RCK = !WDC
# !WRD
# !WLO

enable RWS = TRUE

!RWS = !MC1 & WDC & WRD & WLO
Byte Write Decode PAL B7

Device Location
X6Y35

Device Type
P22V10A

Module
WWB7, flag r1

Revision Date
10/17/88

Declarations
TRUE, FALSE = 1, 0
X, Z, Ck = .X., .Z., .C

GND, VCC
pin 12, 24

MC1, MC0, A0, A1, A2, A3, WRN, WCY
pin 1, 2, 3, 4, 5, 6, 7, 8

WRD, WW1, B7, B6, B5, B4, B3, B2, B1, B0
pin 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Address = [X, X, X, MC1, MC0, A2, A1, A0]

Equations
enable B0 = !WRN & !WCY

!B0 = (Address==^h10)

enable B1 = !WRN & !WCY

!B1 = (Address==^h11)

enable B2 = !WRN & !WCY

!B2 = (Address==^h12)

enable B3 = !WRN & !WCY

!B3 = (Address==^h13)

enable B4 = !WRN & !WCY

!B4 = (Address==^h14)

enable B5 = !WRN & !WCY
!B5 = (Address==^h15)

enable B6 = !WRN & !WCY

!B6 = (Address==^h16)

enable B7 = !WRN & !WCY

!B7 = (Address==^h17)

enable WW1 = !WRN & !WCY

!WW1 = MC0 & MC1
# MC1 & A3

WRD = MC0
# MC1
# WRN
# WCY
Bus Flipper PAL B8

Device Location
All devices on sheets 13-22 of schematic 6450-0565

Device Type
P16R4A

Module
WWB8, flag r0

Revision Date
10/18/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C

GND, VCC
pin 10, 20

CLK, DA, DB, DC, DD, MV, MSK, WTG, WRD
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

OE, WDD, WDC, WD, WC, WB, WA, WDB, WDA
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Equations
enable WDA = WTG

!WDA = !WRD & !DA
# WRD & !MSK & !WA
# WRD & MSK & !MV

enable WDB = WTG

!WDB = !WRD & !DB
# WRD & !MSK & !WB
# WRD & MSK & !MV

!WA:= !WDA

!WB:= !WDB

!WC:= !WDC

!WD:= !WDD

enable WDC = WTG
\!WDC = \!WRD \& \!DC
\# \!WRD \& \!MSK \& \!WC
\# \!WRD \& \!MSK \& \!MV

enable \ WDD = WTG

\!WDD = \!WRD \& \!DD
\# \!WRD \& \!MSK \& \!WD
\# \!WRD \& \!MSK \& \!MV
FIFO Reset Control PAL B9

Device Location
X31Y76, X23Y48

Device Type
P16L8

Module
WWB9, flag r0

Revision Date
11/16/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C

GND, VCC
pin 10, 20

Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, INI
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

GO, R7, R6, R5, R4, R3, R2, R1, R0
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Equations
enable R0 = TRUE

!R0 = !INI
# Q0 & GO

enable R1 = TRUE

!R1 = !INI
# Q1 & GO

enable R2 = TRUE

!R2 = !INI
# Q2 & GO

enable R3 = TRUE

!R3 = !INI
# Q3 & GO

enable R4 = TRUE
!R4 = !INI
# Q4 & GO

enable R5 = TRUE

!R5 = !INI
# Q5 & GO

enable R6 = TRUE

!R6 = !INI
# Q6 & GO

enable R7 = TRUE

!R7 = !INI
# Q7 & GO
Address Range Control PAL B10

Device Location
X14Y4

Device Type
P16L8

Module
WWB10, flag r0

Revision Date
05/02/89

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0

GND, VCC
pin 10, 20

W4, W5, W6, W7, W8, W9, W10, M19, M1A
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

M1B, ARE, M1C, M1D, AOE, M1E, M1F, ACL, CLR
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Equations
enable CLR = TRUE
!CLR = ACL

enable AOE = TRUE
!AOE = W4 & W5 & W6 & W7 & M19 "200 FRAMES
# W4 & !W5 & W6 & W7 & M19 & M1A "300 FRAMES
# W5 & W6 & W7 & M1A "400 FRAMES
# W6 & W7 & M1B "800 FRAMES
# W6 & !W7 & M1B & M1C "1200 FRAMES
# W7 & M1C "1600 FRAMES

enable ARE = TRUE
!ARE = AOE & !M1D & !M1E & !M1F
Interface Board PAL Equations

Memory Decoder/Frame Interrupt PAL C1

Device Location
U1

Device Type
P16L8

Module
WWC1, flag r0

Revision Date
12/07/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 10, 20

A17, A18, A19, A20, A21, A22, A23, M24, INT
pin 1, 2, 3, 4, 5, 6, 7, 8, 9

IRS, IR15, DI, FI, ADL, ALS, INP, DIR, MEM
pin 11, 12, 13, 14, 15, 16, 17, 18, 19

Equations
enable MEM = TRUE

enable DIR = TRUE
!

!DIR = !INP
"DELAY

enable ALS = TRUE

!ALS = ADL

enable FI = TRUE

!FI = INT & DI & IRS
# IRS & !FI
"SET
"HOLD/RESET

enable DI = TRUE

!DI = INT
enable IR15 = !FI

!IR15 = TRUE
Strobe Decoder PAL C2

Device Location
U2

Device Type
P22V10

Module
WWC2, flag r0

Revision Date
12/07/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 12, 24

CMD, S0, S1, MIO, CS, RST, A1, A2, A3, I0, I1
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

MEM, IRS, S16, FBK, RDY, PR, MW, MR, IOW, IOR, INP
pin 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations
!INP = !I1 & !I0 & !MIO & S0 & !S1 & CS & !CMD & !RST
# !MEM & MIO & S0 & !S1 & CS & !CMD & !RST
# !INP & !CMD

!IOR = !I1 & !I0 & !MIO & S0 & !S1 & CS & !CMD
# !IOR & !CMD

!IOW = !I1 & !I0 & !MIO & !S0 & S1 & CS & !CMD
# !IOW & !CMD

!MR = !MEM & MIO & S0 & !S1 & CS & !CMD
# !MR & !CMD

!MW = !MEM & MIO & !S0 & S1 & CS & !CMD
# !MW & !CMD

!PR = RST

enable RDY = !RST

!RDY = !I1 & !I0 & !MIO & S0 & !S1 & CS & CMD
# !MEM & MIO & S0 & !S1 & CS & CMD

9-42

Issued 3/91
enable FBK = !RST

!FBK = !I1 & !I0 & !MIO & CS
  # !MEM & MIO & CS

enable S16 = !RST

!S16 = !I1 & !I0 & !MIO & CS
  # !MEM & MIO & CS

!IRS = RST
  # !I1 & !I0 & !MIO & !A3 & A2 & !A1 & S0 & !S1 & CS & !CMD
  # !IRS & !CMD
Lower Address Latch/Decoder PAL C3

Device Location  U3
Device Type      P22V10
Module           WW3C, flag r0
Revision Date    12/07/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
    pin  12, 24

ADL, BH, A0, A1, A2, A3, A4, A5, A6, A7
    pin  1, 2, 3, 4, 5, 6, 7, 8, 9, 10

IOS0, PA7, PA6, PA5, PA4, PA3, PA2, PA1, PA0, PBH
    pin  14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations
PBH := BH
PA0 := A0
PA1 := A1
PA2 := A2
PA3 := A3
PA4 := A4
PA5 := A5
PA6 := A6
PA7 := A7

##IOS0 = !A7 & !A6 & A5 & A4 & A3  "38H-3FH
# !A7 & !A6 & A5 & A4 & A2  "34H-37H

9-44  Issued 3/91
 Upper Address Latch/Decoder PAL C4

Device Location
U4

Device Type
P22V10

Module
WWC4, flag r0

Revision Date
12/07/88

Declarations
TRUE, FALSE = 1, 0
H, L = 1, 0
X, Z, Ck = .X., .Z., .C.

GND, VCC
pin 12, 24

ADL, A8, A9, A10, A11, A12, A13, A14, A15, A16
pin 1, 2, 3, 4, 5, 6, 7, 8, 9, 10

IOS1, PA16, PA15, PA14, PA13, PA12, PA11, PA10, PA9, PA8
pin 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Equations
PA8 := A8

PA9 := A9

PA10 := A10

PA11 := A11

PA12 := A12

PA13 := A13

PA14 := A14

PA15 := A15

PA16 := A16

A Board Signal Mnemonics

These signal mnemonics are provided to help you trace signal names that enter or exit each sheet of the A Board schematics. The origin and destination columns describe the schematic sheet number (1-33), horizontal grid coordinate (A-D) and vertical grid coordinate (1-8), respectively. For multiple origins and/or destinations, these coordinates are condensed where possible. For example, the WIDE WORD Address Lines (WAD00/WAD31) have origins at 12A,B,C6, 12B,C3. Since two sheet numbers are listed (even though they are the same), there are two sets of coordinates, i.e., 12A,B,C6 and 12B,C3. The first set has a common sheet number (12) and a common vertical coordinate (6), but three horizontal coordinates. Thus, the first set can be expanded to 12A6, 12B6 and 12C6. Likewise, the second set can be expanded to 12B3 and 12C3.

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Signal Name</th>
<th>Origin(s)</th>
<th>Destination(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVR</td>
<td>Channel A Vertical Read</td>
<td>14B1</td>
<td>13B4</td>
</tr>
<tr>
<td>B[0-7]</td>
<td>Blue 0-7</td>
<td>30A1</td>
<td>32B6, 33C8</td>
</tr>
<tr>
<td>BDC</td>
<td>Blue Dual Channel</td>
<td>32C1</td>
<td>1C4</td>
</tr>
<tr>
<td>BI1</td>
<td>Blue Image 1</td>
<td>31D5</td>
<td>1D4</td>
</tr>
<tr>
<td>BI2</td>
<td>Blue Image 2</td>
<td>31D1</td>
<td>1D4</td>
</tr>
<tr>
<td>BINK</td>
<td>Blink Strobe</td>
<td>19C1</td>
<td>6A3, 21A8</td>
</tr>
<tr>
<td>BLANK/</td>
<td>Composite Blanking</td>
<td>3D1</td>
<td>31B8, 31B4, 32B8, 33B8</td>
</tr>
<tr>
<td>BNTSC</td>
<td>Blue NTSC</td>
<td>33C1</td>
<td>1C4</td>
</tr>
<tr>
<td>BRL</td>
<td>Blink Rate Load</td>
<td>2C4</td>
<td>19D3</td>
</tr>
<tr>
<td>B[0-7]</td>
<td>Dual Channel Blue Bus</td>
<td>30A1</td>
<td>32B8, 33C8</td>
</tr>
<tr>
<td>BSA[0-7]</td>
<td>Byte Select Channel A 0-7 (FIFO Read Strobe)</td>
<td>13A2</td>
<td>14A,B,C8</td>
</tr>
<tr>
<td>BSB[0-7]</td>
<td>Byte Select Channel B 0-7 (FIFO Read Strobe)</td>
<td>15A2</td>
<td>16A,B,C8</td>
</tr>
<tr>
<td>BSC[0-7]</td>
<td>Byte Select Channel C 0-7 (FIFO Read Strobe)</td>
<td>17A2</td>
<td>18A,B,C8</td>
</tr>
<tr>
<td>BVR</td>
<td>Channel B Ready</td>
<td>16B1</td>
<td>15B4</td>
</tr>
<tr>
<td>C0HP</td>
<td>Cursor 0 Horizontal Position</td>
<td>2B4</td>
<td>4D8</td>
</tr>
<tr>
<td>C0HS</td>
<td>Cursor 0 Horizontal Size</td>
<td>2B4</td>
<td>4A8</td>
</tr>
<tr>
<td>C0T</td>
<td>Cursor 0 Type</td>
<td>2B4</td>
<td>4A4</td>
</tr>
<tr>
<td>C0VP</td>
<td>Cursor 0 Vertical Position</td>
<td>2B4</td>
<td>4D1</td>
</tr>
<tr>
<td>C0VS</td>
<td>Cursor 0 Vertical Size</td>
<td>2B4</td>
<td>4A1</td>
</tr>
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These signal mnemonics are provided to help you trace signal names that enter or exit each sheet of the B Board schematics. The origin and destination columns describe the schematic sheet number (1-22), horizontal grid coordinate (A-D) and vertical grid coordinate (1-8), respectively. For multiple origins and/or destinations, these coordinates are condensed where possible. For example, the WIDE WORD Address Lines (WAD00-WAD31) have destinations at 12A,B,C,D3. The coordinate set has a common sheet number (12) and a common vertical coordinate (3) but four horizontal coordinates. Thus, this set can be expanded to 12A3, 12B3, 12C3 and 12D3.

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<td>9C4</td>
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<tr>
<td>LDFE</td>
<td>Load Data FIFO E</td>
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<tr>
<td>LFR</td>
<td>Lower FIFO Read</td>
<td>4D8</td>
<td>5C8</td>
</tr>
<tr>
<td>MAF/</td>
<td>Middle FIFO A Full</td>
<td>5C3</td>
<td>6D8</td>
</tr>
<tr>
<td>MBF/</td>
<td>Middle FIFO B Full</td>
<td>5B3</td>
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<td>MBSY/</td>
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</tr>
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<td>MEMR/</td>
<td>Memory Read</td>
<td>2B5</td>
<td>3C4</td>
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<td>MEMW/</td>
<td>Memory Write</td>
<td>2B5</td>
<td>3D4, 4B7</td>
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<td>MSIZ/</td>
<td>Memory Size Buffer</td>
<td>3B1</td>
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<td>PCA0-16</td>
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<td>2B8</td>
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<td>Destination(s)</td>
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<td>----------------</td>
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<tr>
<td>PCINT/</td>
<td>PC Interrupt</td>
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<td>PC Memory Read</td>
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<td>PCRST/</td>
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<td>PL4</td>
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<td>12C1</td>
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<td>PXLCK4</td>
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<td>Readback RAM Data 00-1F</td>
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<tr>
<td>R20-3F</td>
<td>Readback RAM Data 20-3F</td>
<td>18A3</td>
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<td>R40-5F</td>
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<td>R60-7F</td>
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<td>RA0-B</td>
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<td>13D8, 14D8, 15D8, 16D8</td>
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<td>Read Data Bus</td>
<td>Sheets 13, 14, 15 and 16A3</td>
<td>Sheets 17, 18, 19, and 20D8</td>
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<td>RRFR/</td>
<td>Raster Read FIFO Reset</td>
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<td>Read/Write Address</td>
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<td>WIDE WORD Readback Write Strobe</td>
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<td>UFD00-UFD17</td>
<td>FIFOed Data Bus</td>
<td>5D1,2,3</td>
<td>1C,D2</td>
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<td>Vertical Interval</td>
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<td>11A7</td>
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<td>WIDE WORD Address Available</td>
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<td>11B1</td>
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<td>WAF0/</td>
<td>Write Address FIFO 0 Full</td>
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<td>Mnemonic</td>
<td>Signal Name</td>
<td>Origin(s)</td>
<td>Destination(s)</td>
</tr>
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<td>----------</td>
<td>-----------------------------------</td>
<td>-----------</td>
<td>----------------</td>
</tr>
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<td>Write Address FIFO 1 Full</td>
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<td>WAF2/</td>
<td>Write Address FIFO 2 Full</td>
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<td>WAF3/</td>
<td>Write Address FIFO 3 Full</td>
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<td>6B8</td>
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<td>WCLBY/</td>
<td>WIDE WORD Clear Busy</td>
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<td>WD00Q/- WD631/</td>
<td>Bidirectional Write Data Bus</td>
<td>1A,B,C,D5, 1A,B,C,D6, Sheets 13, 14, 15, and 16</td>
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<td>WDC</td>
<td>WIDE WORD Data Accepted</td>
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<td>WDF0/-3/</td>
<td>Write Data FIFOs 0-3 Full</td>
<td>8D6</td>
<td>6C8</td>
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<td>WDF4/-7/</td>
<td>Write Data FIFOs 4-7 Full</td>
<td>8D1</td>
<td>6C8</td>
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<td>WDF8/-B/</td>
<td>Write Data FIFOs 8-B Full</td>
<td>9D6</td>
<td>6C8</td>
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<td>WDFC/-F/</td>
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<td>9D1</td>
<td>6C8</td>
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<td>WDTAC/</td>
<td>WIDE WORD Data Acknowledge</td>
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<td>11C1</td>
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<td>WDTRQ/</td>
<td>WIDE WORD Data Request</td>
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<td>WINT/</td>
<td>WIDE WORD Initialization</td>
<td>1D8</td>
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<td>WLO/</td>
<td>WIDE WORD Lock Out</td>
<td>11C8</td>
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<td>WMBSY/</td>
<td>WIDE WORD Memory Busy</td>
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<td>11A7</td>
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<td>WIDE WORD Memory Interrupt</td>
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<td>11A8</td>
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<td>WRA/</td>
<td>Stretched Write/Read Enable</td>
<td>11A1</td>
<td>10B6, 12D6</td>
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<td>WRD</td>
<td>Write Data</td>
<td>10A3</td>
<td>11B1, 13D8, 14D8, 15D8, 16D8</td>
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<tr>
<td>WREAD/</td>
<td>WIDE WORD Read</td>
<td>11B1</td>
<td>1C8</td>
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<tr>
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<td>10C6</td>
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<tr>
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<td>Write/Read Enable</td>
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<td>11A7</td>
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<td>WIDE WORD Size 00/-11/</td>
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<td>WWB07/</td>
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<tr>
<td>WWBW1/</td>
<td>WIDE WORD Bus Word</td>
<td>10B3</td>
<td>1C8</td>
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# McIDAS Design Note 46: WIDE WORD McIDAS Memory and Port Bit Map

**Revision Date**: 11/29/88  
**Rev. Level**: A  
**Original Date**: 09/26/88  
**Design Note**: DN 3504-046

## Input Port 33CH

<table>
<thead>
<tr>
<th>Bit</th>
<th>WIDE WORD Memory Size</th>
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<td>2</td>
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<td>3</td>
<td>WWS3</td>
</tr>
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<td>4</td>
<td>WWS4</td>
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<td>9</td>
<td>WWS9</td>
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<tr>
<td>A</td>
<td>WWSA</td>
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<td>B</td>
<td>WWSB</td>
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**Cursor Enhancement**

<table>
<thead>
<tr>
<th>C</th>
<th>Command FIFO empty</th>
</tr>
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<tr>
<td>D</td>
<td>Command FIFO half full</td>
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**WIDE WORD Write Data**

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<th>E</th>
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<tbody>
<tr>
<td>F</td>
<td>Data FIFO half full</td>
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## Input Port 33EH

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<tr>
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<td>Middle command FIFO overflow</td>
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<td>2</td>
<td>Upper command FIFO overflow</td>
</tr>
<tr>
<td>3</td>
<td>Command address FIFO overflow</td>
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### WIDE WORD Data Write

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<td>4</td>
<td>Lower data byte overflow</td>
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<tr>
<td>5</td>
<td>Upper data byte overflow</td>
</tr>
<tr>
<td>6</td>
<td>Address overflow</td>
</tr>
<tr>
<td>7</td>
<td>Readback RAM load complete</td>
</tr>
<tr>
<td></td>
<td>(reset by RAM read)</td>
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<table>
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<th>Bit</th>
<th>Notation</th>
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<tr>
<td>E</td>
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</tr>
<tr>
<td>F</td>
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## Output Port 336H

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<th>0-64K Memory Segment (0-F)</th>
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<td>3</td>
<td>SEG 3</td>
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### Output Port 338H

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<td>LLA</td>
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<td>LLC</td>
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### Output Port 33AH

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<td>B</td>
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<td>E</td>
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**Output Port 33CH**

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<thead>
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</tr>
<tr>
<td>3</td>
<td>Bit Plane 3</td>
</tr>
<tr>
<td>4</td>
<td>Bit Plane 4</td>
</tr>
<tr>
<td>5</td>
<td>Bit Plane 5</td>
</tr>
<tr>
<td>6</td>
<td>Bit Plane 6</td>
</tr>
<tr>
<td>7</td>
<td>Bit Plane 7</td>
</tr>
<tr>
<td>8</td>
<td>Address Count Direction (high=up)</td>
</tr>
<tr>
<td>9</td>
<td>Mode Control 0*</td>
</tr>
<tr>
<td>A</td>
<td>Mode Control 1*</td>
</tr>
<tr>
<td>B</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
</tr>
</tbody>
</table>

*MC1 MC0

0 0 Write 16 pixel groups
0 1 Read 16 pixel groups
1 0 Write pixel/bit plane
1 1 Erase pixel/bit plane segment

**Output Port 33EH**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Upper Address Segment For Memory Writes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ADR 10</td>
</tr>
<tr>
<td>1</td>
<td>ADR 11</td>
</tr>
<tr>
<td>2</td>
<td>ADR 12</td>
</tr>
<tr>
<td>3</td>
<td>ADR 13</td>
</tr>
<tr>
<td>4</td>
<td>ADR 14</td>
</tr>
<tr>
<td>5</td>
<td>ADR 15</td>
</tr>
<tr>
<td>6</td>
<td>ADR 16</td>
</tr>
<tr>
<td>7</td>
<td>ADR 17</td>
</tr>
<tr>
<td>8</td>
<td>ADR 18</td>
</tr>
<tr>
<td>9</td>
<td>ADR 19</td>
</tr>
<tr>
<td>A</td>
<td>ADR 1A</td>
</tr>
<tr>
<td>B</td>
<td>ADR 1B</td>
</tr>
<tr>
<td>C</td>
<td>ADR 1C</td>
</tr>
<tr>
<td>D</td>
<td>ADR 1D</td>
</tr>
<tr>
<td>E</td>
<td>ADR 1E</td>
</tr>
<tr>
<td>F</td>
<td>ADR 1F</td>
</tr>
</tbody>
</table>
Line Write

1. Load Upper Address Segment: 16 bits, Port 33E_H I/O
2. Load Mode: zero all 16 bits, Port 33C_H I/O
3. Load pixels: 64-128K address range, Modulo 16 Start Address, as groups of 16 pixels in sequence

Readback

1. Load Upper Start Address Segment: 16 bits, Port 33E_H I/O
2. Load Mode: bit 9 set high, bit 8 is the read direction where 0 = address decrement and 1 = address increment, all other bits low, Port 33C_H I/O
3. Load Transfer Length: 16 bits at Modulo 16 Start Address
4. Wait For Transfer Done Bit: Status Bit 7, Port 33E_H I/O
5. Read desired pixels: 64-128K address range

Byte Write

1. Load Upper Address Segment: 16 bits, Port 33E_H I/O
2. Load Mode and Change Mask: Port 33C_H I/O, bits 0-7 = bit planes 0-7, high = change, bit A is high, bits 8, 9, B-F are low
3. Load Value at Pixel Address: Byte Write, bits 0-7 = bit planes 0-7, 64-128K address range

Erase Segment

1. Load Upper Start Address: 16 bits, Port 33E_H I/O
2. Load Mode and Erase Mask: Port 33C_H I/O bits 0-7 = bit planes 0-7, high = erase, bit 8 = erase direction where low = decrement and high = increment, bits 9 and A are high
3. Load Number of lines to erase: bits 0-7, Port 33A_H
4. Load Line Length: 16 bits, Port 338_H
5. Load Erase Value: Byte Write, bits 0-7 = bit planes 0-7, Modulo 16
Start Address, address range 64-128K

### 0-64K Segment 0 (Port 336H=0)

<table>
<thead>
<tr>
<th>ADR (HEX)</th>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>SLW FS/UH CH.0</td>
<td>SLW = Start Lower Word</td>
</tr>
<tr>
<td>100</td>
<td>SLW LH CH.0</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>SLW FS/UH CH.1</td>
<td>FS = Full Screen</td>
</tr>
<tr>
<td>300</td>
<td>SLW LH CH.1</td>
<td>LH = Lower Half</td>
</tr>
<tr>
<td>400</td>
<td>SLW FS/UH CH.2</td>
<td>UH = Upper Half</td>
</tr>
<tr>
<td>500</td>
<td>SLW LH CH.2</td>
<td>(16 bits)</td>
</tr>
<tr>
<td>600</td>
<td>VERT SWITCH LINE</td>
<td>(9 bits)</td>
</tr>
<tr>
<td>700</td>
<td>HORIZ SWITCH PIXEL</td>
<td>(10 bits)</td>
</tr>
<tr>
<td>800</td>
<td>SUW FS/UH CH.0</td>
<td>SUW = Start Upper Word</td>
</tr>
<tr>
<td>900</td>
<td>SUW LH CH.0</td>
<td></td>
</tr>
<tr>
<td>A00</td>
<td>SUW FS/UH CH.1</td>
<td></td>
</tr>
<tr>
<td>B00</td>
<td>SUW LH CH.1</td>
<td>(16 bits)</td>
</tr>
<tr>
<td>C00</td>
<td>SUW FS/UH CH.2</td>
<td></td>
</tr>
<tr>
<td>D00</td>
<td>SUW LH CH.2</td>
<td></td>
</tr>
<tr>
<td>E00</td>
<td>DISPLAY MODE</td>
<td>(16 bits)</td>
</tr>
<tr>
<td>F00</td>
<td>BLINK RATE</td>
<td>(8 bits)</td>
</tr>
<tr>
<td>1000</td>
<td>LL FS/UH CH.0</td>
<td>LL = Line Length (of area, 16-bit Modulo 16 value)</td>
</tr>
<tr>
<td>1100</td>
<td>LL LH CH.0</td>
<td></td>
</tr>
<tr>
<td>1200</td>
<td>LL FS/UH CH.1</td>
<td></td>
</tr>
<tr>
<td>1300</td>
<td>LL LH CH.1</td>
<td></td>
</tr>
<tr>
<td>1400</td>
<td>LL FS/UH CH.2</td>
<td></td>
</tr>
<tr>
<td>1500</td>
<td>LL LH CH.2</td>
<td></td>
</tr>
<tr>
<td>1600</td>
<td>CH.0 MASK</td>
<td>(16 bits)</td>
</tr>
<tr>
<td>1700</td>
<td>CH.1 MASK</td>
<td>(16 bits)</td>
</tr>
<tr>
<td>1800</td>
<td>ZF FS/UH CH.0</td>
<td>ZF = Zoom Factor (0-15, 4-bit)</td>
</tr>
<tr>
<td>1900</td>
<td>ZF LH CH.0</td>
<td></td>
</tr>
<tr>
<td>1A00</td>
<td>ZF FS/UH CH.1</td>
<td></td>
</tr>
<tr>
<td>1B00</td>
<td>ZF LH CH.1</td>
<td></td>
</tr>
<tr>
<td>1C00</td>
<td>ZF FS/UH CH.2</td>
<td></td>
</tr>
<tr>
<td>1D00</td>
<td>ZF LH CH.2</td>
<td></td>
</tr>
<tr>
<td>1E00</td>
<td>CH.2 MASK</td>
<td>(16 bits)</td>
</tr>
<tr>
<td>1F00</td>
<td>DC MASK</td>
<td>(16 bits)</td>
</tr>
<tr>
<td>Address</td>
<td>Function</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------------------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>2000-210F</td>
<td>LABEL #</td>
<td></td>
</tr>
<tr>
<td>2100-220F</td>
<td>CUR 0 HORIZ. POSITION</td>
<td></td>
</tr>
<tr>
<td>2200-230F</td>
<td>CUR 0 VERT. POSITION</td>
<td></td>
</tr>
<tr>
<td>2300-240F</td>
<td>CUR 0 HORIZ. SIZE</td>
<td></td>
</tr>
<tr>
<td>2400-250F</td>
<td>CUR 0 VERT SIZE</td>
<td></td>
</tr>
<tr>
<td>2500-260F</td>
<td>CUR 0 TYPE</td>
<td></td>
</tr>
<tr>
<td>2600-270F</td>
<td>CUR 1 HORIZ POSITION</td>
<td></td>
</tr>
<tr>
<td>2700-280F</td>
<td>CUR 1 VERT POSITION</td>
<td></td>
</tr>
<tr>
<td>2800-290F</td>
<td>CUR 1 HORIZ SIZE</td>
<td></td>
</tr>
<tr>
<td>2900-2A0F</td>
<td>CUR 1 VERT SIZE</td>
<td></td>
</tr>
<tr>
<td>2A00-407F</td>
<td>CUR 1 TYPE</td>
<td></td>
</tr>
<tr>
<td>4000-417F</td>
<td>FS/UH LABEL #1</td>
<td>(~106 character displayed)</td>
</tr>
<tr>
<td>4080-417F</td>
<td>FS/UH LABEL #2</td>
<td>FS=Full Screen</td>
</tr>
<tr>
<td>4100-417F</td>
<td>FS/UH LABEL #3</td>
<td>UH = Upper Half</td>
</tr>
<tr>
<td>4F80-5FF</td>
<td>FS/UH LABEL #32</td>
<td></td>
</tr>
<tr>
<td>5000-507F</td>
<td>LH LABEL #1</td>
<td>LH = Lower Half</td>
</tr>
<tr>
<td>5080-5FF</td>
<td>LH LABEL #2</td>
<td></td>
</tr>
<tr>
<td>5F80-5FF</td>
<td>LH LABEL #32</td>
<td></td>
</tr>
</tbody>
</table>
## Enhancement Tables

<table>
<thead>
<tr>
<th>Port 336H Value</th>
<th>0-64K MEM Address Range</th>
<th>Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>7000-7FFF</td>
<td>CH.0 Red</td>
</tr>
<tr>
<td>0</td>
<td>8000-8FFF</td>
<td>CH.0 Green</td>
</tr>
<tr>
<td>0</td>
<td>9000-9FFF</td>
<td>CH.0 Blue</td>
</tr>
<tr>
<td>0</td>
<td>A000-AFFF</td>
<td>CH.1 Red</td>
</tr>
<tr>
<td>0</td>
<td>B000-BFFF</td>
<td>CH.1 Green</td>
</tr>
<tr>
<td>0</td>
<td>C000-CFFF</td>
<td>CH.1 Blue</td>
</tr>
<tr>
<td>0</td>
<td>D000-DFFF</td>
<td>CH.2 Red</td>
</tr>
<tr>
<td>0</td>
<td>E000-EFFF</td>
<td>CH.2 Green</td>
</tr>
<tr>
<td>0</td>
<td>F000-FFFF</td>
<td>CH.2 Blue</td>
</tr>
<tr>
<td>1</td>
<td>0-FFFF</td>
<td>DUAL Red</td>
</tr>
<tr>
<td>2</td>
<td>0-FFFF</td>
<td>DUAL Green</td>
</tr>
<tr>
<td>3</td>
<td>0-FFFF</td>
<td>DUAL Blue</td>
</tr>
</tbody>
</table>

R-G-B load sequence; 4K maximum of Red, Green, and Blue per vertical interval.

## Cursor Constructs

<table>
<thead>
<tr>
<th>Port 336H Value</th>
<th>0-64K MEM Address Range</th>
<th>Cursor</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0-FFFF</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0-FFFF</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0 of byte; low = off, high = on
Masks CH.0, CH.1, CH.2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>VB0</td>
</tr>
<tr>
<td>1</td>
<td>VB1</td>
</tr>
<tr>
<td>2</td>
<td>VB2</td>
</tr>
<tr>
<td>3</td>
<td>VB3</td>
</tr>
<tr>
<td>4</td>
<td>VB4</td>
</tr>
<tr>
<td>5</td>
<td>VB5</td>
</tr>
<tr>
<td>6</td>
<td>VB6</td>
</tr>
<tr>
<td>7</td>
<td>VB7</td>
</tr>
<tr>
<td>8</td>
<td>Cursor 0</td>
</tr>
<tr>
<td>9</td>
<td>Cursor 1</td>
</tr>
<tr>
<td>A</td>
<td>Label Enable</td>
</tr>
<tr>
<td>B</td>
<td>Blink Enable</td>
</tr>
<tr>
<td>C</td>
<td>Full/Upper Blank *</td>
</tr>
<tr>
<td>D</td>
<td>Lower Blank *</td>
</tr>
<tr>
<td>E</td>
<td>Full/Left Blank *</td>
</tr>
<tr>
<td>F</td>
<td>Right Blank *</td>
</tr>
</tbody>
</table>

* Control Ch. 1 and Ch. 2 inputs to 16-bit table also.

16-Bit Table Mask

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>CH.1 VB0</td>
</tr>
<tr>
<td>1</td>
<td>CH.1 VB1</td>
</tr>
<tr>
<td>2</td>
<td>CH.1 VB2</td>
</tr>
<tr>
<td>3</td>
<td>CH.1 VB3</td>
</tr>
<tr>
<td>4</td>
<td>CH.1 VB4</td>
</tr>
<tr>
<td>5</td>
<td>CH.1 VB5</td>
</tr>
<tr>
<td>6</td>
<td>CH.1 VB6</td>
</tr>
<tr>
<td>7</td>
<td>CH.1 VB7</td>
</tr>
<tr>
<td>8</td>
<td>CH.2 VB0</td>
</tr>
<tr>
<td>9</td>
<td>CH.2 VB1</td>
</tr>
<tr>
<td>A</td>
<td>CH.2 VB2</td>
</tr>
<tr>
<td>B</td>
<td>CH.2 VB3</td>
</tr>
<tr>
<td>C</td>
<td>CH.2 VB4</td>
</tr>
<tr>
<td>D</td>
<td>CH.2 VB5</td>
</tr>
<tr>
<td>E</td>
<td>CH.2 VB6</td>
</tr>
<tr>
<td>F</td>
<td>CH.2 VB7</td>
</tr>
</tbody>
</table>
Blink Rate

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>BR0</td>
</tr>
<tr>
<td>1</td>
<td>BR1</td>
</tr>
<tr>
<td>2</td>
<td>BR2</td>
</tr>
<tr>
<td>3</td>
<td>BR3</td>
</tr>
<tr>
<td>4</td>
<td>BR4</td>
</tr>
<tr>
<td>5</td>
<td>BR5</td>
</tr>
<tr>
<td>6</td>
<td>BR6</td>
</tr>
<tr>
<td>7</td>
<td>BR7</td>
</tr>
</tbody>
</table>

Blink rate = 30Hz / N + 1
where N = 0 - 255

Cursor Type

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>CT0</td>
</tr>
<tr>
<td>1</td>
<td>CT1</td>
</tr>
<tr>
<td>2</td>
<td>CT2</td>
</tr>
</tbody>
</table>

where:

0 = Off
1 = Box
2 = Crosshair
3 = Box and crosshair
4 = Solid box
5 = Star Wars gun sight
6 = Construct From Memory
7 = Solid Background Window Construct
Cursor Horizontal Position

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>5</td>
<td>32</td>
</tr>
<tr>
<td>6</td>
<td>64</td>
</tr>
<tr>
<td>7</td>
<td>128</td>
</tr>
<tr>
<td>8</td>
<td>256</td>
</tr>
<tr>
<td>9</td>
<td>512</td>
</tr>
</tbody>
</table>

Cursor Horizontal Size (Half Width)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>5</td>
<td>32</td>
</tr>
<tr>
<td>6</td>
<td>64</td>
</tr>
<tr>
<td>7</td>
<td>128</td>
</tr>
</tbody>
</table>

\[
\text{HORIZ CENTER} = \text{HPOS} + \text{HSIZE} + \text{OFFSET}
\]

OFFSET  HPOS      HSIZE
<---128--->

DISPLAY START
(640 pixels)
Cursor Vertical Position

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>5</td>
<td>32</td>
</tr>
<tr>
<td>6</td>
<td>64</td>
</tr>
<tr>
<td>7</td>
<td>128</td>
</tr>
<tr>
<td>8</td>
<td>256</td>
</tr>
</tbody>
</table>

Cursor Vertical Size (Half Height)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>5</td>
<td>32</td>
</tr>
<tr>
<td>6</td>
<td>64</td>
</tr>
<tr>
<td>7</td>
<td>128</td>
</tr>
</tbody>
</table>

VERT CENTER = VPOS + VSIZE + OFFSET

```
43
OFFSET

DISPLAY  START (480 LINES)

VPOS

VSIZE
```
Roaming Off A Frame Edge

Left Horizontal

IF: Display Start Point < Frame Start Point

THEN: Horizontal Switch Point = Frame Start Point - Display Start Point

AND: Left Horizontal Blank = On

Right Horizontal

IF: Display Start Point > (Frame Start Point + Line Length - 640/Zoom Factor)

THEN: Horizontal Switch Point = 640 - (Display Start Point -- (Frame Start Point + Line Length-640/Zoom Factor))

AND: Right Horizontal Blank = On

Left

BLANKED

| ------------------ | ------------------ | DISPLAYED VIDEO |---------|
| DISP | FRAME | DISP |
| START | EDGE | END |
| (START) |

Right

BLANKED

| ------------------ | DISPLAYED VIDEO | --------- | ------------------ |
| DISP | FRAME | DISP |
| START | EDGE | END |
| (START + LINE LENGTH) |

Issued 3/91
Vertical Top

IF: (Frame Start Point - Display Start Point) > Line Length

THEN: Vertical Switch Point = Integer ((Frame Start Point - Display Start Point) / Line Length)

AND: Vertical Top Blanking = On

Vertical Bottom

IF: Display Start Point > "Frame End Point - 480/Zoom Factor"

THEN: Vertical Switch Point = 480 -- Integer ((Display Start Point - (Frame End Point - 480/Zoom Factor))

AND: Vertical Bottom Blanking = On

*Frame End Point = Frame Start Point + (Line Length x number of lines in the frame)
Frame Description

6-32  Bit Start Addresses; 2 per channel for top and bottom paneling
6-16  Bit (Modulo 16) Length; 2 per channel for top and bottom paneling
6-4   Bit Zoom Factor (0-15); 2 per channel

Panel Select

10 bits  Horizontal Switch Point
9 bits   Vertical Switch Point
3 bits   Paneling Mode: Off, Vert, Horiz, Quad, and Stereo
         Frame Interleave
12 bits  Panel Enhancement Mode, 3 bits per panel; Graphics
         On/off, Ch. 1, Ch. 2, Nortle

Cursor Description (2 Sets for 2 Cursors)

10 bits  Horizontal Center Point
9 bits   Vertical Center Point
8 bits   Horizontal Size (half width)
7 bits   Vertical Size (half height)
3 bits   Cursor Type

Label Line

64 lines (32 for top; 32 for bottom) of 128 characters (~106 characters show)
ASCII characters written into 8K address space
Read Select
   6 bits Line Select
   1 bit Label Display Enable
## Segment 0 Address C00E00

### Display Mode Mask

<table>
<thead>
<tr>
<th>Mask Code</th>
<th>Description</th>
<th>Video Description</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>LOWER RIGHT CH.2 VIDEO</td>
<td>Bottom Vertical Split</td>
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<tr>
<td>1</td>
<td>LOWER RIGHT CH.1 VIDEO</td>
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<tr>
<td>2</td>
<td>LOWER LEFT CH.2 VIDEO</td>
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<tr>
<td>3</td>
<td>LOWER LEFT CH.1 VIDEO</td>
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<tr>
<td>4</td>
<td>UPPER RIGHT CH.2 VIDEO</td>
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<td>6</td>
<td>UPPER LEFT CH.2 VIDEO</td>
<td>Full Screen</td>
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<td>7</td>
<td>UPPER LEFT CH.1 VIDEO</td>
<td>Full Screen</td>
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<td>8</td>
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<tr>
<td>B</td>
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<tr>
<td>C</td>
<td>DISPLAY MODE CONTROL 0</td>
<td>Display Mode</td>
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<tr>
<td>D</td>
<td>DISPLAY MODE CONTROL 1</td>
<td>Display Mode</td>
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<tr>
<td>E</td>
<td>DISPLAY MODE CONTROL 2</td>
<td>Display Mode</td>
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<tr>
<td>F</td>
<td>WINDOW CURSOR 2</td>
<td>H = Window</td>
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### Display Mode

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<tr>
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<td>VERT PANELS</td>
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<td>2</td>
<td>HORIZ PANELS</td>
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<tr>
<td>3</td>
<td>QUAD PANELD</td>
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<tr>
<td>4</td>
<td>ALTERNATE FRAME</td>
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<tr>
<td>5</td>
<td>SPLIT ALTERNATE FRAME</td>
</tr>
<tr>
<td>6</td>
<td>3 VIDEO CHANNELS</td>
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<tr>
<td>7</td>
<td>SPLIT 3 VIDEO CHANNELS</td>
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### Graphic

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<th>B</th>
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<tr>
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<table>
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<tr>
<th>7/6</th>
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<tbody>
<tr>
<td>3/2</td>
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<td>1/0</td>
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